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Thyristor trigger circuit for a reversible d.c. motor drive with regenerative braking

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UDC 621.316.718:621.316.719.3:621.313.223:621.382.333.4

The trigger circuit for a reversible d.c. motor drive is described. The drive uses a three-phase twin thyristor bridge to allow regenerative braking to be used. The trigger circuit is constructed from 61 series circuit modules with a minimum of external components. The effects of temperature and mains voltage variations on the control characteristic are described.

INTRODUCTION

One of the best-known and well-established systems for regenerative motor control in use at present is the Ward-Leonard system. This is an electromechanical system. The advantages of static control equipment using thyristors for the speed or torque control of d.c. motors are well known. The fully static Ward-Leonard system with controlled braking and reversing extends the advantages of static drive into more specialised fields.

A previous article (Ref. 1) described the basis of a design for a reversible drive with regenerative braking based on the Ward-Leonard system. The design was taken as far as determining the various units necessary for the operation of the drive, and work is in progress on the detailed design of these units. This article describes the trigger circuit—the interface between the sensing and logic switching units of the controller and the semiconductor devices required to control the power to the motor. The trigger circuit uses the recently introduced 61 series of circuit modules, and has been designed so that only passive components are used outside the modules, while the number of redundant semiconductor devices inside the modules is kept to a minimum. The power that can be controlled by the drive depends on the thyristor stack used, and systems of this type can be constructed to control motors of up to at least 100hp.

BASIC SYSTEM DESIGN

The motor speed-control system consists essentially of five sections, as shown in Fig. 1. These sections are: the controller, the phase-shift trigger circuit, the current limit circuit, the thyristor twin-bridge stack, and the d.c. shunt motor. The three feedback loops used are also shown in Fig. 1.

Input/output requirements for trigger circuit

The connections required between the trigger circuit and the rest of the system are shown in Fig. 1. A 0 to 5V control signal v_c determines the motor speed by control of the armature voltage, while the clockwise and anti-clockwise signals V_{cw} and V_{ccw} determine the direction of rotation of the motor shaft.

The output of the trigger circuit delivers a train of pulses to the thyristors through pulse transformers. The pulse trains are accurately synchronised to the three-phase mains supply. The output pulses are suitable for triggering all Mullard thyristors; the published data for the 61 series modules give information for triggering other devices.

Trigger circuit

The trigger circuit controls two three-phase fully controlled bridges connected in inverse-parallel across the motor load, as shown in Fig. 2. The direction of rotation of the motor shaft is determined by selecting either Bridge A or Bridge B with the signals V_{cw} or V_{ccw}. These bridge selection signals must never be applied together, otherwise a short-circuit will result across the mains supply. A minimum interval of approximately 20ms must be allowed between the selection of the bridges.

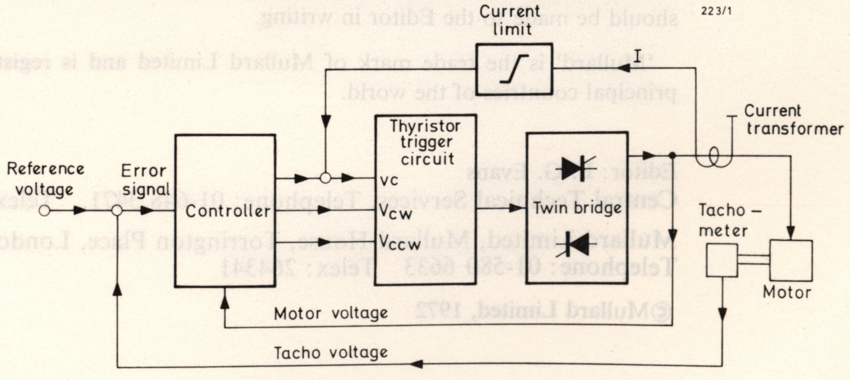


Fig. 1—Block diagram of motor speed-control system

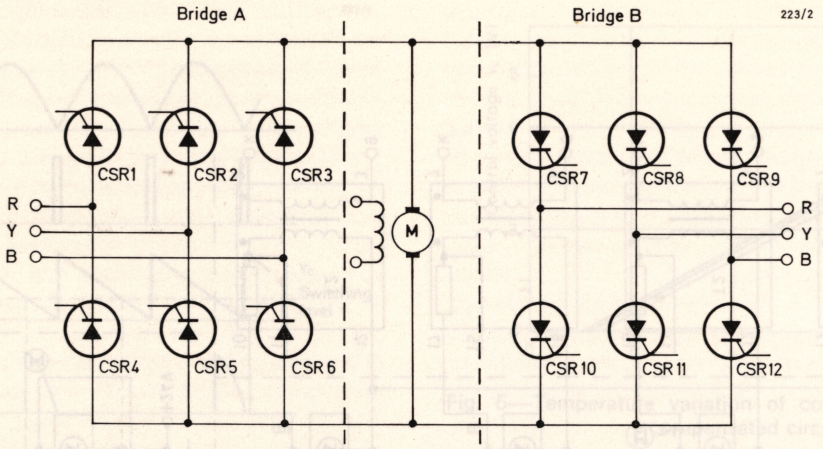


Fig. 2—Thyristor twin-bridge circuit with motor

The trigger circuit consists of three twin-bridge trigger units (TBTU). Each unit controls the thyristors of a particular phase in both bridges, and is constructed from seven circuit modules and some passive components mounted on a printed-wiring board. One TBTU has an additional module to generate a continuous train of pulses. The functions and module types for one TBTU are listed below.

Output stage	4×UPA61
Phase-shift stage	1×UPA61
Synchronising bistable	1×2NOR61
D.C. supply	1×RSA61
Pulse generator	1×UPA61

In addition to the three printed-wiring boards, six TT61 trigger transformers are required.

The continuous train of pulses from the pulse generator is synchronised by gating circuits in each TBTU to ensure that the appropriate thyristors in the bridge receive pulses simultaneously. The repetition frequency of the generator is 10kHz, and the pulses have a duration of 20μs.

Adjustment for maximum and minimum trigger angle is provided on each TBTU to obtain correct balancing of the three line currents. The minimum conduction angle (that is, the highest trigger angle) must be set at a fixed value when there is zero input control voltage, say 20 to 30 degrees. This is to provide 'end stop' pulses which are required to ensure commutation of the thyristors when the system is regenerating. In the regenerating condition, the motor appears as a d.c. source and the regenerating bridge as an inverter which is commutated by the mains supply. The d.c. current flowing in one thyristor will be commutated by another thyristor in the bridge so long as trigger pulses are available. If one thyristor was not commutated, the result would be a short-circuit across the motor causing a high circulating current to flow, limited only by the low armature resistance.

CIRCUIT DESCRIPTION

The circuit diagram of one twin-bridge trigger unit is shown in Fig. 3. Waveforms at the points marked with roman numerals in Fig. 3 are shown in Fig. 4.

A synchronised full-wave supply waveform (I) is obtained from the diodes in the RSA61 module, as shown in Fig. 3. This synchronised signal is applied to the base of a UPA61 output transistor. At the zero voltage points of the mains supply, a 220nF capacitor is charged to a zener voltage of 6·8V (waveform II), and discharged linearly by a constant-current circuit (see Appendix 1). The 10kΩ variable resistor determines the rate of discharge. The ramp waveform (III) is applied to a Schmitt trigger circuit through an emitter follower. When the ramp voltage reaches the Schmitt 'off' level, the transistor connected to the output of the Schmitt trigger removes the diode clamping at the input of the 2NOR61 gates. A part of the supply waveform (IV and V) is thus applied to the inputs of the 2NOR61 gates arranged as a bistable. The resultant bistable output waveforms, Q_1 (waveform VI) and Q_2 (waveform VII), will be 180° out of phase, with the Schmitt 'off' level determining the phase relationship between Q_1, Q_2, and the mains supply.

The outputs Q_1 and Q_2 from another TBTU are applied to inputs X_1 (waveform VIII) and X_2 (waveform IX) to limit the length of the trigger pulse train to a 120° period. The pulses from a pulse generator (see Appendix 2) (waveform X) are applied with the Q and X signals to transistor gates controlling the four UPA61 output stages.

The master pulse generator is switched on by the application of a +24V signal on the V_s input, as shown in Fig. 3. Similarly, a +24V signal is applied to V_{ccw} to control two thyristors in Bridge A (outputs A and $\bar{A}$, waveforms XI and XII), or to V_{cw} to control two thyristors in Bridge B (outputs B and $\bar{B}$).

The control voltage v_c is applied to the base of an emitter follower whose output v_c' is connected to the common

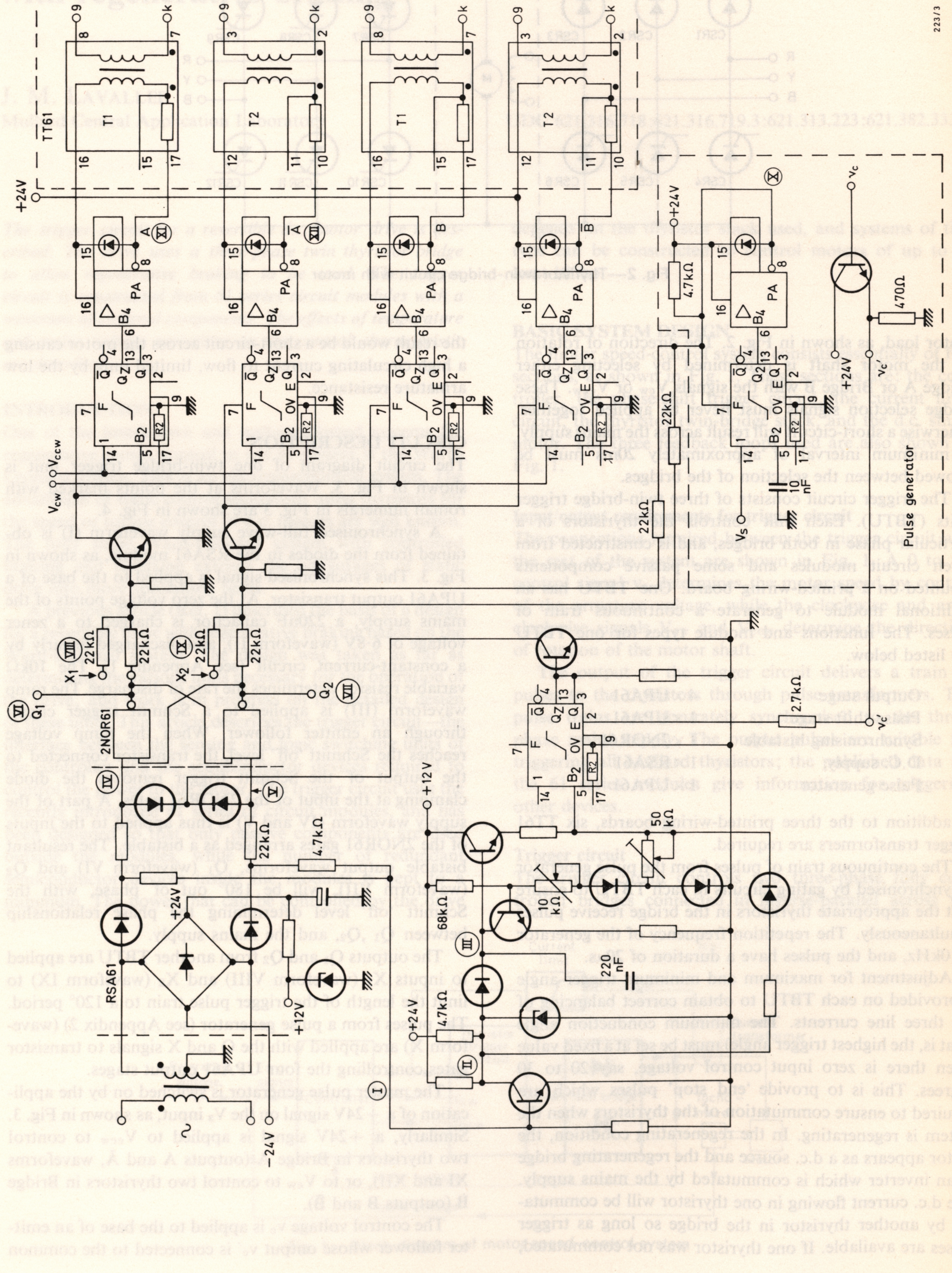


Fig. 3—Circuit diagram of twin-bridge trigger unit. The roman numerals refer to the waveforms of Fig. 4

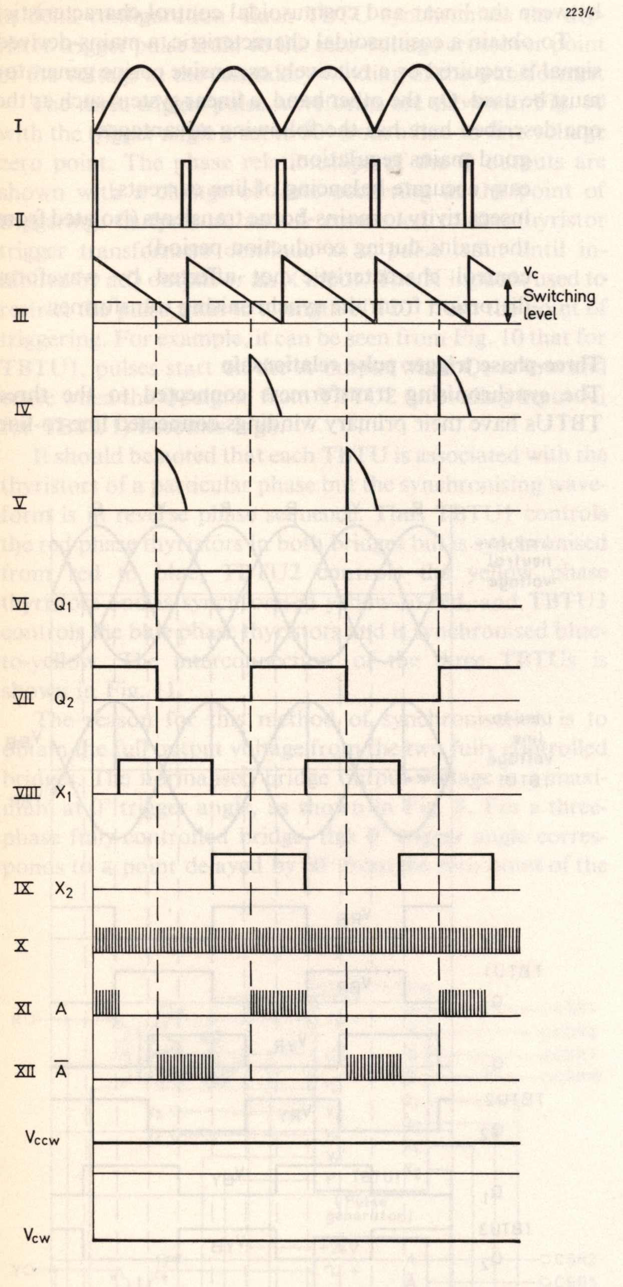


Fig. 4—Waveforms in twin-bridge trigger unit. The roman numerals refer to the points in the circuit of Fig. 3 at which the waveforms are obtained

emitter point of the Schmitt trigger circuit to control the switch-off level, which determines the trigger pulse train phase relationship.

Temperature and mains supply stabilisation

The principal sources of error due to temperature variation are in the ramp discharge and the Schmitt trigger circuits. Temperature compensation is obtained by using the change in diode V_{be} to control the ramp discharge and Schmitt trigger level. Two diodes in series are used for the ramp discharge circuit and one for the Schmitt trigger circuit. These diodes are available from the 2NOR61 module. The effect of temperature variation on the trigger pulse phase shift for the compensated circuit is shown in Fig. 5.

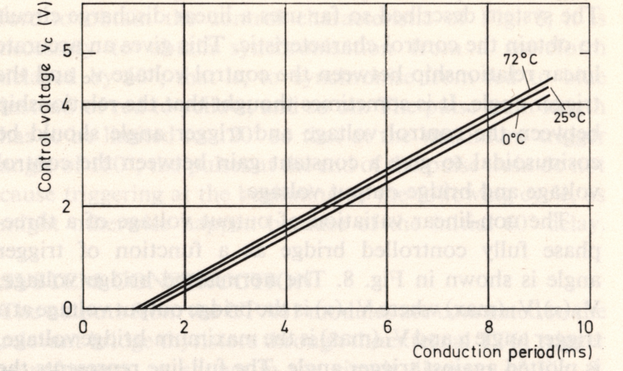


Fig. 5—Temperature variation of control characteristic for compensated circuit

In regenerative systems, variations of the mains supply must not affect the control characteristic. The voltage characteristic for this system is shown in Fig. 6 where the trigger angle variation of one bridge must correspond inversely to the trigger angle variation of the other bridge. Any change in the control characteristic will cause an asymmetrical relationship between the motoring and generating quadrants of the system. The effect of supply voltage variation on the control characteristic is shown in Fig. 7 to be very small.

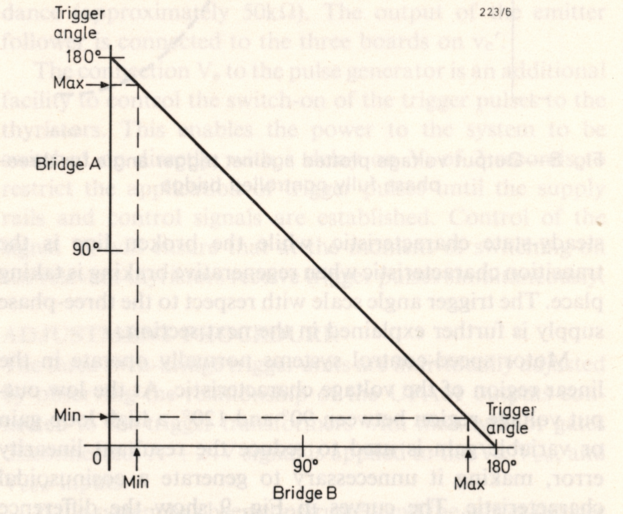


Fig. 6—Trigger angle relationship for twin thyristor bridges

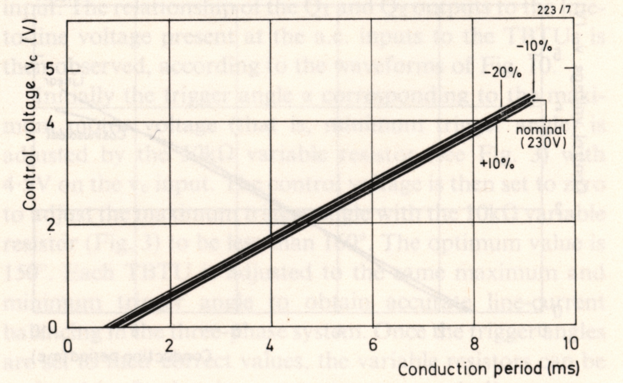


Fig. 7—Supply voltage variation of control characteristic

Linear or cosinusoidal control

The system described so far uses a linear discharge circuit to obtain the control characteristic. This gives an accurate linear relationship between the control voltage v_c and the trigger angle. It is sometimes thought that the relationship between the control voltage and trigger angle should be cosinusoidal to give a constant gain between the control voltage and bridge output voltage.

The non-linear variation of output voltage of a three-phase fully controlled bridge as a function of trigger angle is shown in Fig. 8. The normalised bridge voltage, $V_B(\alpha)/V_B(\text{max})$ where $V_B(\alpha)$ is the bridge output voltage at a trigger angle α and $V_B(\text{max})$ is the maximum bridge voltage, is plotted against trigger angle. The full line represents the steady-state characteristic, while the broken line is the transition characteristic when regenerative braking is taking place. The trigger angle scale with respect to the three-phase supply is further explained in the next section.

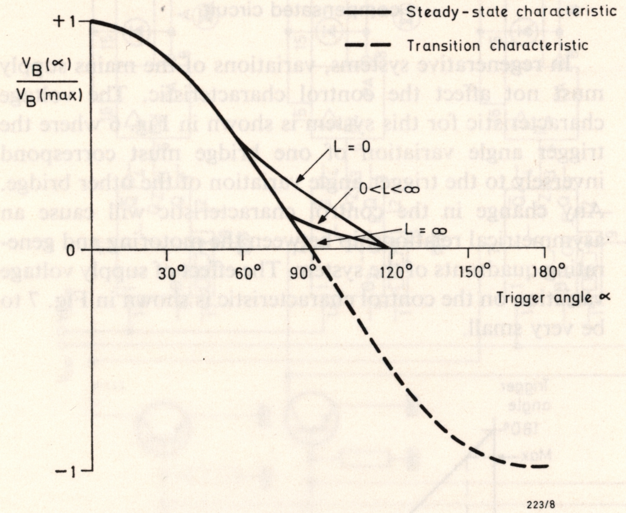


Fig. 8—Output voltage plotted against trigger angle for three-phase fully controlled bridge

Motor speed-control systems normally operate in the linear region of the voltage characteristic. At the low output voltage region between 90° and 120°, a high loop gain or variable gain is used to reduce the resultant linearity error, making it unnecessary to generate a cosinusoidal characteristic. The curves in Fig. 9 show the difference between the linear and cosinusoidal control characteristic.

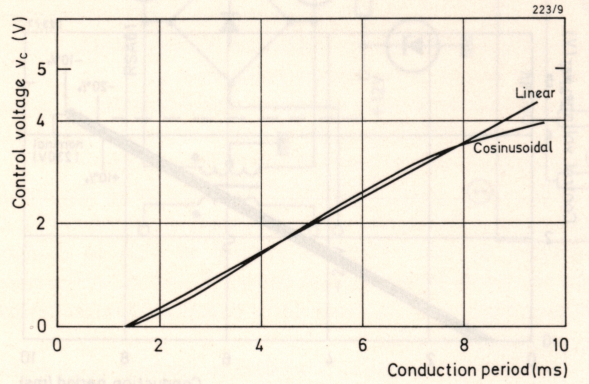


Fig. 9—Linear and cosinusoidal control characteristics

To obtain a cosinusoidal characteristic, a mains-derived signal is required or a relatively expensive cosine generator must be used. On the other hand, a linear system such as the one described here has the following advantages:

good mains regulation,
easy accurate balancing of line currents,
insensitivity to mains-borne transients (isolated from the mains during conduction period),
control characteristic not affected by waveform distortion from the synchronising transformer.

Three-phase trigger pulse relationship

The synchronising transformers connected to the three TBTUs have their primary windings connected line-to-line in delta configuration. Each TBTU synchronises the thyristor trigger pulse train to the zero-voltage crossover point of the voltage at the secondary winding of the transformer.

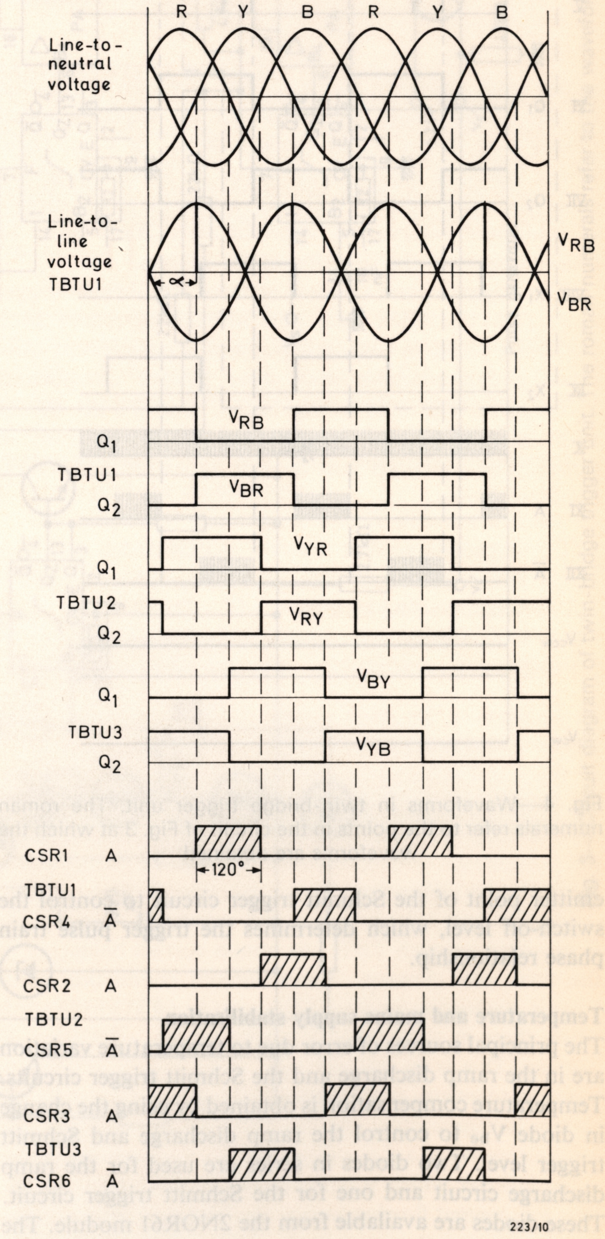


Fig. 10—Trigger pulse relationships for Bridge A at trigger angle of 90°

The three trigger pulse waveforms are shown in Fig. 10 with the trigger angle α set to 90° from a line-to-line voltage zero point. The phase relationships of the Q outputs are shown with a change of state occurring at the point of triggering. Outputs A and Ā connected to the thyristor trigger transformers continue as a pulse train until inhibited by a Q output or an X input. The X input is used to restrict the pulse train to a length of 120° from the point of triggering. For example, it can be seen from Fig. 10 that for TBTU1, pulses start on the A output when Q_1 is low and cease when the Q_2 signal from TBTU2 (providing input X_1 for TBTU1) becomes high.

It should be noted that each TBTU is associated with the thyristors of a particular phase but the synchronising waveform is in reverse phase sequence. Thus TBTU1 controls the red phase thyristors in both bridges but is synchronised from red to blue, TBTU2 controls the yellow phase thyristors and is synchronised yellow-to-red, and TBTU3 controls the blue phase thyristors and is synchronised blue-to-yellow. The interconnection of the three TBTUs is shown in Fig. 11.

The reason for this method of synchronisation is to obtain the full output voltage from the two fully controlled bridges. The normalised bridge output voltage is a maximum at 0° trigger angle, as shown in Fig. 8. For a three-phase fully controlled bridge, this 0° trigger angle corresponds to a point delayed by 60° from the zero point of the line-to-line voltage taken in three-phase sequence. Therefore to obtain the control characteristic of Fig. 8, it is necessary to obtain synchronisation from a waveform delayed by 60°; that is, to synchronise from red to blue instead of red to yellow, and so on. The pulse train length has to be limited to 120° so that at the maximum trigger angle of 180°, the pulses at the end of the pulse train do not cause triggering at the beginning of the following cycle, as might otherwise happen because of the initial 60° delay.

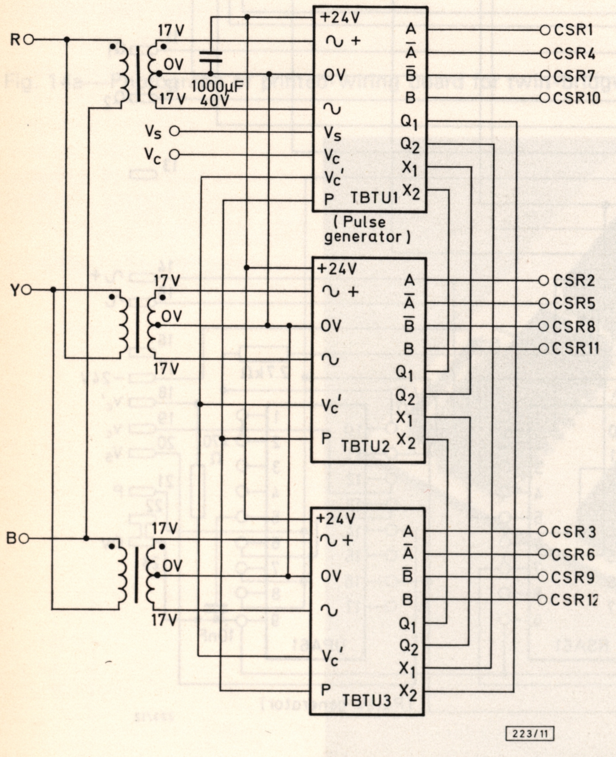


Fig. 11—Interconnection of twin-bridge trigger units

SYSTEM CONSTRUCTION

The outputs from the UPA61 modules are connected to the relevant bridge thyristors through the external TT61 trigger transformers, as shown in the circuit diagram of Fig. 3. The connections from the TBTUs to the thyristors of the two three-phase bridges are shown in Fig. 11. It is important that the polarity of the synchronising transformers is as shown in Fig. 11. For example, when the voltage V_{RB} is positive, the voltage on pin 1 of the RSA61 module is also positive.

The +24V rails from the RSA61 modules are interconnected. The pulse output from the pulse generator is applied to the P terminals on the other two boards. The interconnections of the Q and X signals are also shown in Fig. 11.

The control voltage v_c is applied to an emitter follower in the pulse generator module to provide a high input impedance (approximately 50kΩ). The output of the emitter follower is connected to the three boards on v_c'.

The connection V_s to the pulse generator is an additional facility to control the switch-on of the trigger pulses to the thyristors. This enables the power to the system to be switched on directly, with a delay on V_s of 2 seconds to restrict the application of trigger pulses until the supply rails and control signals are established. Control of the signal V_s will ensure that at the moment of switching-on the relevant thyristors receive trigger pulses simultaneously.

ADJUSTMENT PROCEDURE

The three twin-bridge trigger units are individually adjusted by observing the relationship of the UPA61 outputs connected to the trigger transformers with the thyristor gates disconnected. A +24V signal is applied to the V_s, V_{cw}, and V_{ccw} inputs.

If the system has been constructed and the power devices already connected, however, the system can be set up if there is no signal applied to the pulse generator on the V_s input. The relationship of the Q_1 and Q_2 outputs to the line-to-line voltage present at the a.c. inputs to the TBTUs is then observed, according to the waveforms of Fig. 10.

Initially the trigger angle α corresponding to the maximum motor voltage (that is, minimum trigger angle) is adjusted by the 50kΩ variable resistor (see Fig. 3) with 4·5V on the v_c input. The control voltage is then set to zero to adjust the maximum trigger angle with the 10kΩ variable resistor (Fig. 3) to be less than 160°. The optimum value is 150°. Each TBTU is adjusted to the same maximum and minimum trigger angle to obtain accurate line-current balancing in the three-phase system. Once the trigger angles are set to their correct values, the variable resistors can be replaced by fixed resistors to prevent any misalignment.

COMPONENTS AND PRINTED-WIRING BOARD

The interconnection wiring diagram of the modules and the components of one printed-wiring board for a twin-phase trigger unit is shown in Fig. 12. This unit includes the module forming the pulse generator which is not included on the other two boards. The associated 10nF capacitor and 470Ω resistor are also not required on the other two boards.

A suggested layout for the printed-wiring board is shown in Fig. 13 (wiring side) and Fig. 14 (component side). The board is standardised for rack mounting in a Norbit 2 chassis MC60 38240.

The components required for one twin-bridge trigger unit are listed below.

Modules

UPA61	six
RSA61	one
2NOR61	one

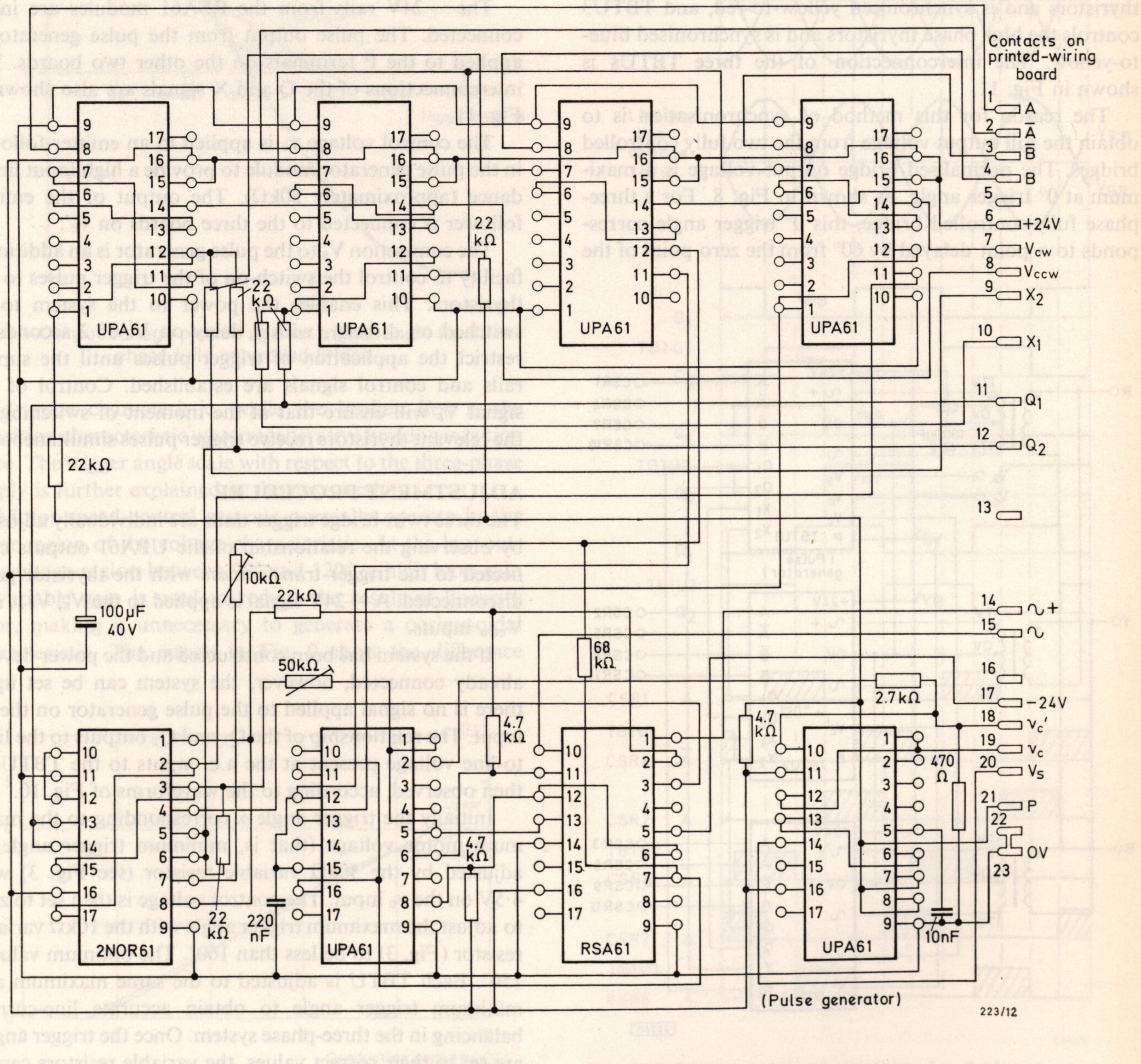
Capacitors

100μF 40V, C437AR/G100	one
220nF 250V, C280AE/P220K	one
10nF 250V, C280AE/P10K	one

Resistors

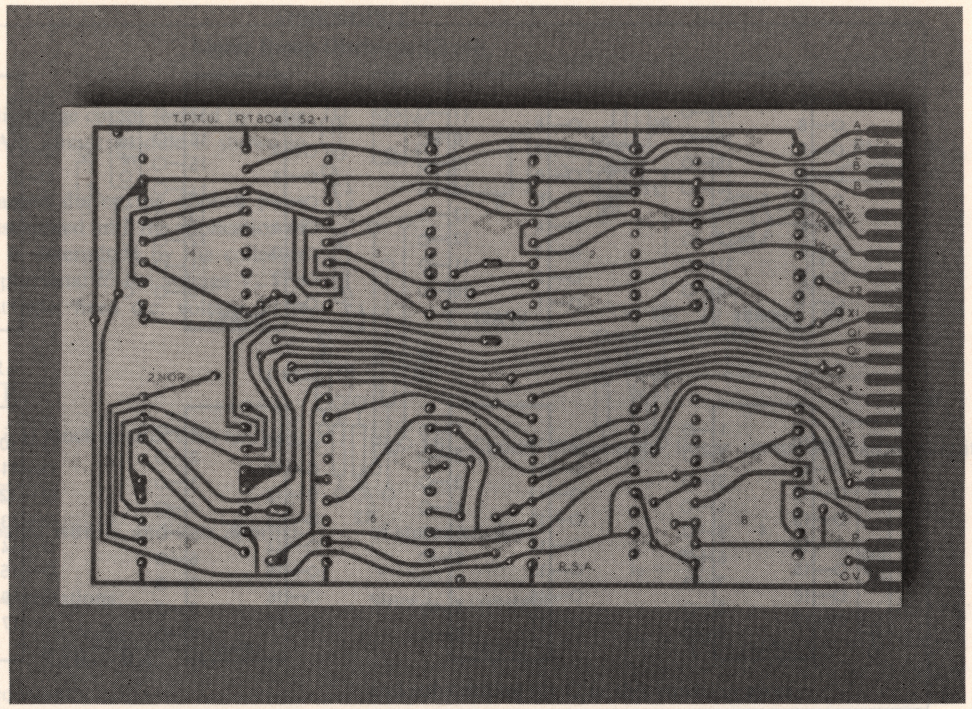
68kΩ, CR25	one
22kΩ, CR25	eight
4·7kΩ, CR25	three
2·7kΩ, CR25	one
470Ω, CR25	one

The positions R_1 and R_2 on the board are for the fixed-value resistors that replace the 10kΩ variable resistor shown in the circuit diagram of Fig. 3 and used for adjusting the maximum trigger angle. Similarly, positions R_3 and R_4 are for the fixed resistors to replace the 50kΩ variable resistor for adjusting the minimum trigger angle.



Contacts on printed-wiring board
1 A
2 A̅
3 B̅
4 B
5
6 +24V
7 Vcw
8 Vccw
9 X2
10 X1
11 Q1
12 Q2
13
14 ∿+
15 ∿
16
17 −24V
18 Vc'
19 Vc
20 Vs
21 P
22
23 0V
UPA61
UPA61
UPA61
UPA61
2NOR61
UPA61
RSA61
UPA61
22 kΩ
22 kΩ
22kΩ
10kΩ
22kΩ
100μF 40V
50kΩ
68 kΩ
2.7kΩ
4.7 kΩ
4.7 kΩ
4.7 kΩ
470 Ω
22 kΩ
220 nF
10nF
(Pulse generator)
223/12

Fig. 12—Interconnection wiring diagram for twin-bridge trigger unit (including pulse generator)



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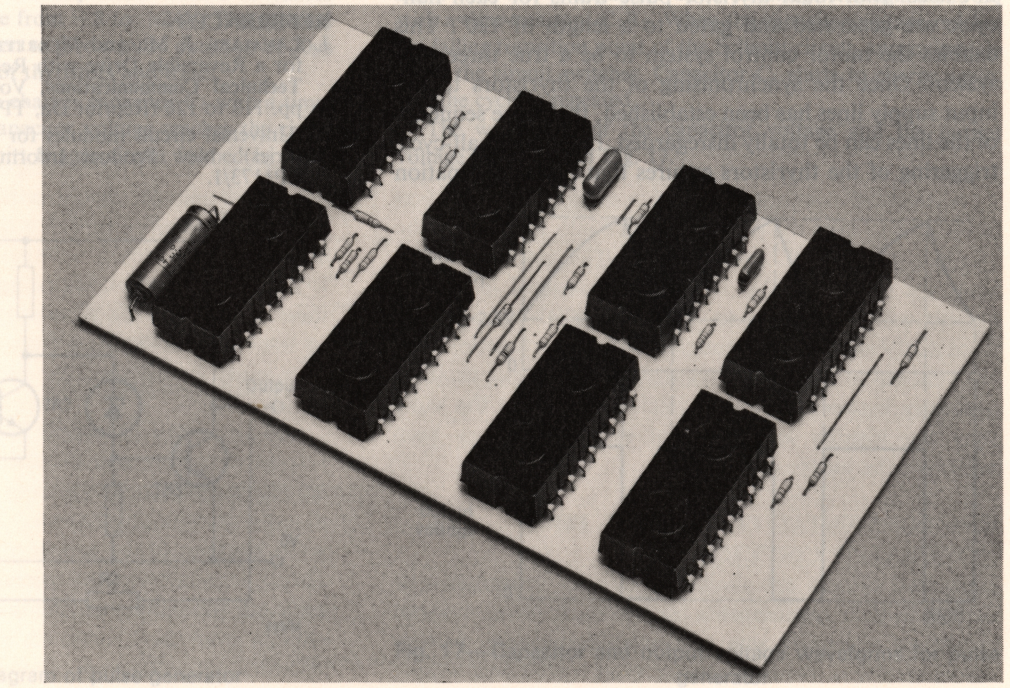
2 NOR
R.S.A.

Fig. 13—Printed-wiring board for twin-bridge trigger unit, wiring side

Fig. 14a—Photograph of printed-wiring board for twin-bridge trigger unit showing layout of components



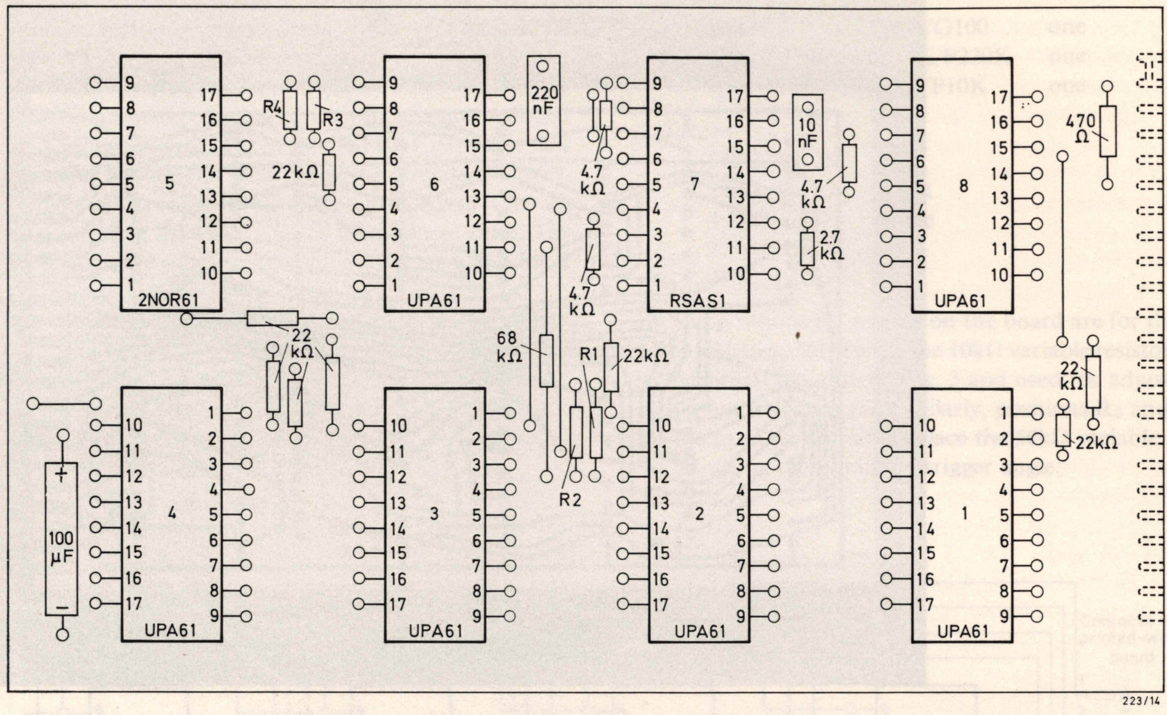


Fig. 14b—Printed-wiring board for twin-bridge trigger unit, layout of components

CONCLUSIONS

The thyristor trigger circuit just described has been specially designed for a three-phase twin-bridge regenerative system. Emphasis has been laid on accurate control, ease of construction, and low cost. The system could also be used for other highly inductive loads requiring rapid decay and reversal of the load current; for example, power supplies.

A highly desirable feature of this system is that the normal method of extending the length of the trigger pulse train beyond the half-cycle by cross-coupling the outputs is not used. Individual thyristor pulse trains for each half-cycle are generated and gated to a length of 120°. This enables the motor control system to be a true three-wire system. Once the synchronising of the thyristors to the input supply lines has been established, the phase sequence of the lines can be totally disregarded. Individual half-cycle triggering of the thyristors ensures that device dissipation during the reverse half-cycle of the mains supply is minimised.

Although the trigger circuit has been specifically designed for three-phase supplies, a single-phase regenerative system can also be constructed with the same printed-wiring boards. The required output power from a thyristor stack will determine the type of mains supply. One printed-wiring board with its pulse generator and four TT61 modules can drive two inverse-parallel single-phase fully controlled bridges.

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2. 'Universal circuit modules for thyristor trigger systems (61 series)'. New Product Information, Mullard Ltd., 1970, TP1173/1.

APPENDIX 1
Linear Ramp Discharge Circuit

The circuit of the linear ramp discharge circuit formed by some of the components of the UPA61 circuit module is shown in Fig. 15 (Ref. 2).

Capacitor C_1 is rapidly charged during the applied pulse through diode D_1, and slowly discharged until the application of a further pulse. The discharge is determined by the collector current i_c, which in turn is proportional to the voltage V_s. To determine the collector current i_c, a fixed d.c. voltage V_s is applied so that:

$$\text{base voltage} = V_{in} = \frac{V_s R_2}{R_1 + R_2},$$

neglecting i_b and assuming that i_s is much greater than i_b. Also:

$$i_c = \frac{V_{in} - V_{be}}{R_3},$$

assuming that i_b is small compared with i_e, and i_c is approximately equal to i_e.

Therefore from the above two equations:

$$i_c = \left(\frac{V_s R_2}{R_1 + R_2} - V_{be}\right) \Big/ R_3 = \frac{V_s R_2}{R_3(R_1 + R_2)} - \frac{V_{be}}{R_3}.$$

Since V_{be} is approximately constant:

$$i_c \propto V_s.$$

Therefore if V_s is kept constant, i_c will be constant.

The charge stored in the capacitor is:

$$Q = v_c \times C_1,$$

and the discharge current i_c is proportional to the rate of change of stored energy:

$$i_c = \frac{dQ}{dt}.$$

Since i_c is constant:

$$i_c = \frac{Q}{t},$$

and substituting for Q in this equation gives:

$$i_c t = v_c C_1,$$

from which:

$$t \propto v_c.$$

Thus the capacitor voltage is directly proportional to time, and the discharge rate is directly proportional to the applied voltage V_s.

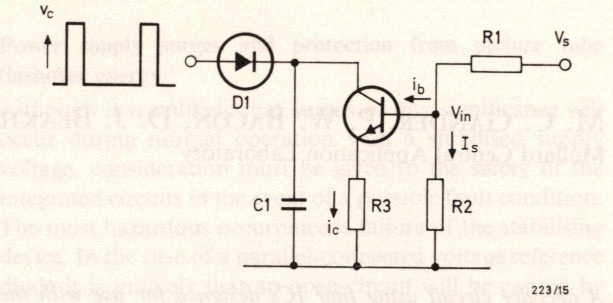

Fig. 15—Circuit diagram of linear ramp discharge circuit

APPENDIX 2
Pulse Generator

The circuit of the pulse generator formed from the UPA61 module is shown in Fig. 16 (Ref. 2). This is a variable-frequency relaxation oscillator with a constant pulse duration output. The frequency variation is approximately linear from 2 to 12kHz with an input control voltage from +8 to +24V. The external capacitor C_1 of 10nF is chosen to give a pulse duration of 20μs to ensure reliable triggering of thyristors and triacs.

The input control voltage charges capacitor C_1 with a time-constant C_1R_1. When the capacitor voltage reaches the rising transition point of the Schmitt trigger circuit formed by transistors TR_1 and TR_2, approximately 6V, the circuit switches. The collector voltage of transistor TR_2 rises towards +24V, and the output transistor TR_3 becomes saturated. This transistor then allows capacitor C_1 to discharge through diode D_1 with a time-constant C_1R_2. When the capacitor voltage reaches the falling transition point of the Schmitt circuit, approximately 2·5V, the circuit switches. Capacitor C_1 starts to charge again, and the cycle is repeated.

The waveforms of the capacitor voltage and the output voltage are shown in Fig. 17.

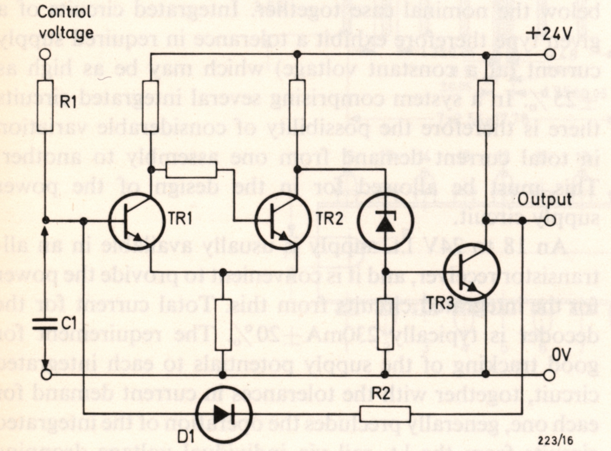

Fig. 16—Circuit diagram of pulse generator

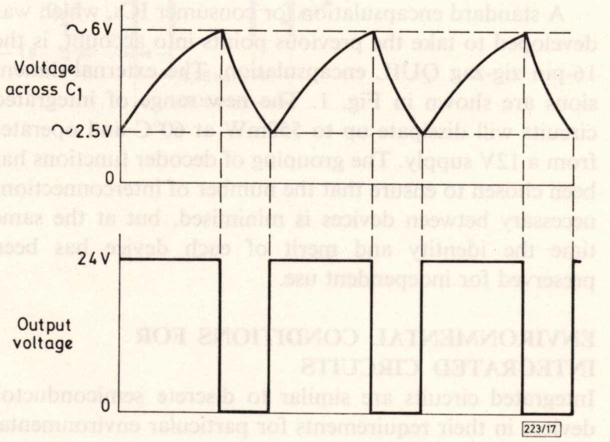

Fig. 17—Capacitor and output voltage waveforms for pulse generator

Colour decoder using integrated circuits

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A decoder circuit using four ICs designed for use with the PAL system is described. It processes the luminance and chrominance signals to give the Red, Green and Blue outputs to the tube. The alignment procedure is also described. The circuit can be assembled on a printed circuit board measuring 230×170mm.

INTRODUCTION

This article describes a complete colour decoder using established PAL techniques and employing four integrated circuits, TBA530, TBA540, TBA560 and TBA990. It processes the signal from the video source to the inputs of the RGB output stages. The controls are d.c. operated to simplify the wiring and user operation of the receiver controls, and to allow complete remote control of the colour receiver if required. The general requirements for an integrated circuit decoder are discussed first.

FUNCTIONAL PARTITIONING

Several considerations influence the way a functional block is divided up between several integrated circuits. The compromise which must be made involves the following:

1) Power dissipation in the device.
2) Heat dissipation aids incorporated in the envelope (such aids increase cost).
3) Chip area.
4) Number of external connecting pins.
5) Production yield figures.
6) Cost of manufacture.

A standard encapsulation for consumer ICs, which was developed to take the previous points into account, is the 16-pin zig-zag QUIL encapsulation. The external dimensions are shown in Fig. 1. The new range of integrated circuits will dissipate up to 550mW at 60°C and operates from a 12V supply. The grouping of decoder functions has been chosen to ensure that the number of interconnections necessary between devices is minimised, but at the same time the identity and merit of each device has been preserved for independent use.

ENVIRONMENTAL CONDITIONS FOR INTEGRATED CIRCUITS

Integrated circuits are similar to discrete semiconductor devices in their requirements for particular environmental conditions to ensure safe and reliable operation in television receivers. Ambient temperature variations, supply voltage variations, and protection against voltage surges and picture tube flashover energy, require similar consideration in either case. However, there are certain special requirements for integrated circuits, particularly where several devices may be used together in a receiver.

Power supplies

The design of each of the integrated circuits allows at least ±10% voltage range over which correct operation is maintained. As a general design approach most of the signal amplitudes, d.c. levels and control functions associated with each integrated circuit track proportionately with voltage. In general, this approach, compared with one in which each critical signal level and d.c. potential is stabilised, results in a smaller chip area for a given functional block and thus a lower cost for the ICs. However, in a receiver with well-stabilised picture tube supply potentials, an operational variation of ±10% in supply voltage to the integrated circuits is likely to result in unacceptable picture variations. Because of operational variations of mains voltage, ambient temperature, and picture tube beam current, an l.t. supply having a voltage stability tolerance of ±3% is recommended to ensure a high degree of picture stability. In any design however, the operational variations, added to the set-to-set spread in supply voltage, should lie within ±10% of the nominal supply voltage.

Unlike groups of discrete components, where the total supply current consumption is the result of an average of the effects of a number of components, all the components of the same kind in an integrated circuit can vary above or below the nominal case together. Integrated circuits of a given type therefore exhibit a tolerance in required supply current (at a constant voltage) which may be as high as ±25%. In a system comprising several integrated circuits there is therefore the possibility of considerable variation in total current demand from one assembly to another. This must be allowed for in the design of the power supply circuit.

An 18 to 24V l.t. supply is usually available in an all-transistor receiver, and it is convenient to provide the power for the integrated circuits from this. Total current for the decoder is typically 230mA±20%. The requirement for good tracking of the supply potentials to each integrated circuit, together with the tolerances in current demand for each one, generally precludes the operation of the integrated circuits from the l.t. rail via individual voltage dropping resistors. Furthermore, similar operation but with a common voltage dropping resistor would also be unacceptable because of the possibility of a combination of one high current integrated circuit with a number of low current ones. The result could be that the voltage across all the circuits would be considerably higher than nominal and excessive power dissipation could occur in the high current one.

These considerations lead to the requirement for:

1) A simple supply source having adequate voltage stability and low impedance, or
2) a resistor feed with a single parallel voltage reference diode connected across the integrated circuits, or
3) a series stabiliser employing a transistor with a voltage reference diode.

For (1), a direct scan-rectified 12V supply could be obtained from the line output transformer in an all-transistor receiver. Such a supply would have voltage variations due to beam current of typically 0·6V for 90° deflection circuits and 0·3V for 110°. However, a diode, an electrolytic capacitor, and an extra transformer tap would be required as well as flashover protection components, and so this is not necessarily the most attractive solution. A possible solution for (1) which does not suffer from variations in voltage due to beam current variations would be from a winding on the line driver transformer. An adequately-rated driver transistor would have to be chosen and the effects of tolerances in drive waveform ratio on the supply voltage should be assessed. For (2), a single voltage reference diode of about 2W dissipation would be required with a ±5% voltage tolerance, and for (3) a series transistor (BD131) regulated by a small voltage reference diode and possibly a preset potentiometer. Solution (2) has been used in the decoder circuit described here.

Power supply surges and protection from picture tube flashover energy

Although it is unlikely that surges of any significance will occur during normal operation with a stabilised supply voltage, consideration must be given to the safety of the integrated circuits in the event of a possible fault condition. The most hazardous occurrence is failure of the stabilising device. In the case of a parallel-connected voltage reference diode it is unlikely that an open-circuit will be caused by damage; a short-circuit is more likely. Where a series stabiliser transistor is employed, which could, for example, be overloaded by a short-circuit on the 12V line, a combination of a series current limiting resistor and a transistor that will not be damaged by the surge current gives adequate protection.

Generally, the integrated circuits will not be affected by surges in supply voltage up to 50% higher than the nominal, provided that each surge is limited to about 20s duration.

Integrated circuits require the same attention to design and layout as discrete transistors to ensure adequate protection against circulating currents caused by picture tube flashover discharges. Where pulses from the line and field timebases are employed for the various gating functions, the layout of the associated networks and the types of components used must not permit the transfer of sharp voltage spikes. Similar attention must be given to the power supply

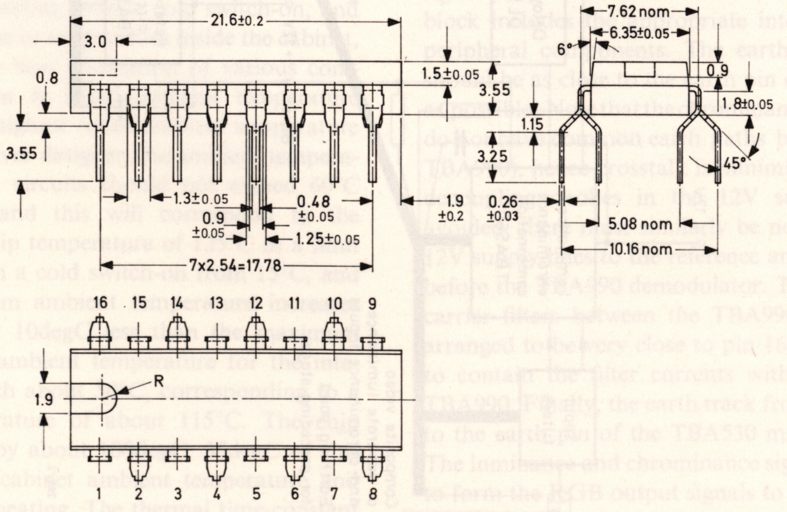

Fig. 1—16-pin zig-zag QUIL encapsulation

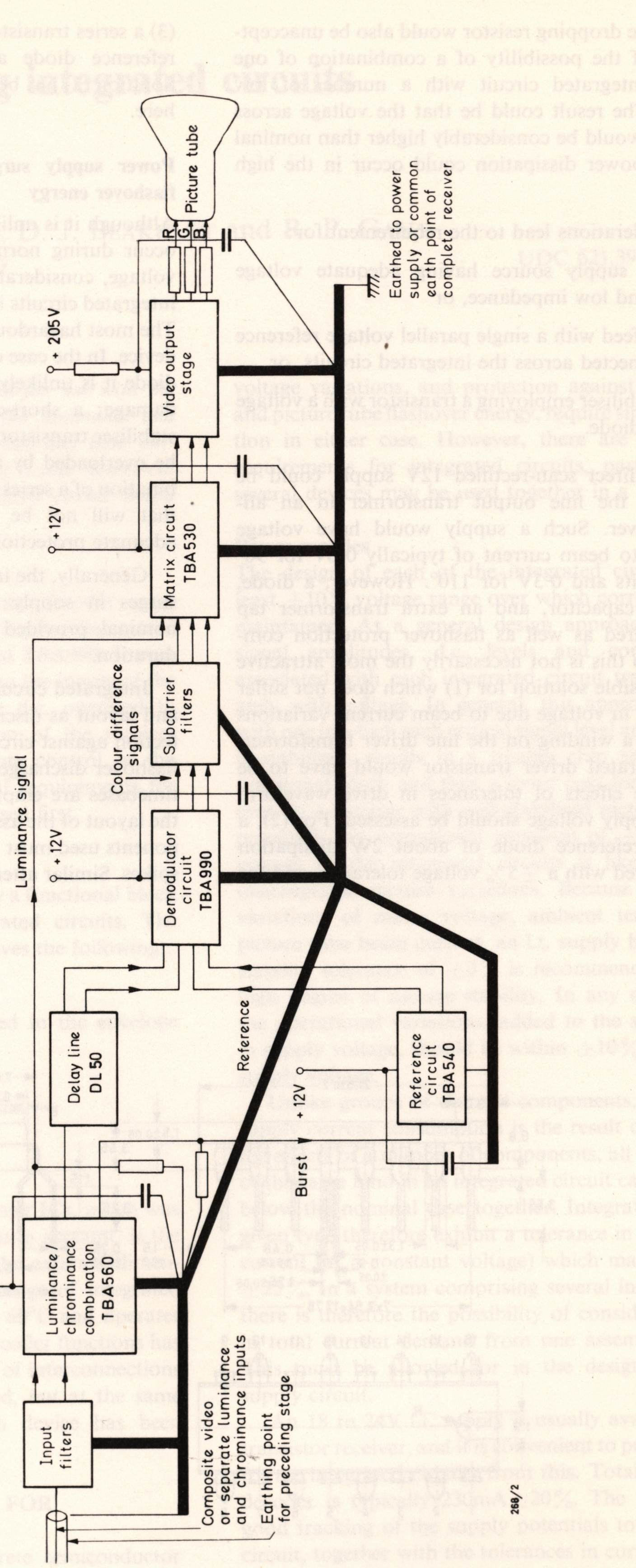
Picture tube
R
G
B
+205V
Video output stage
Earthed to power supply or common earth point of complete receiver
+12V
Matrix circuit TBA530
Subcarrier filters
Colour difference signals
Luminance signal
+12V
Demodulator circuit TBA990
Delay line DL50
Reference
+12V
Reference circuit TBA540
Burst
+12V
Luminance / chrominance combination TBA560
Input filters
Composite video or separate luminance and chrominance inputs
Earthing point for preceding stage
268/2

Fig. 2—Earthing arrangements for decoder circuit

network, particularly if this is derived from the line output transformer.

As with any semiconductor circuitry it is of prime importance to ensure that any wires or cableforms which carry control potentials or signals associated with the integrated circuits are kept away from the picture tube. The external aquadag coating and the P band of the picture tube can be dangerous sources of flashover energy. A particular situation which must be avoided is where the channel selection mechanism and receiver controls are mounted on a panel closely adjacent to the P band. A clearance of at least 30mm between such metalwork and the P band is recommended and the control wiring must be positively located in such a way that it cannot come close to any part of the picture tube. A further precaution of a series resistor, situated close to the IC, is recommended to be connected to any long lead to ensure complete protection against flashover effects. For normal d.c. control leads a value of 1kΩ is appropriate. However in the case of long leads carrying pulses or signals, a lower value may be necessary to avoid waveform distortion. Provided that the leads in such cases are not excessively long, a value of 100Ω gives useful protection. Each integrated circuit should have a bypass capacitor (typically 100nF, metallised-film type) connected close to its supply pins to give stability and isolation at high frequency. These capacitors also increase the protection of the integrated circuits against flashover effects.

Heat considerations

With the l.t. supply voltage stabilised at 12V, each integrated circuit is permitted to operate up to a cabinet ambient temperature of 60°C. Non-stabilised operation with the possibility of a ±10% rise in supply voltage permits operation up to 55°C.

Any drifts in operation of the integrated circuit because of temperature are due to two main causes. These are (1), chip warm-up by self-heating from a cold switch-on, and (2) the relatively slow rise in temperature inside the cabinet, which is caused by the heat dissipation of various components, and variations in room ambient temperature during viewing. In the highest room ambient temperature allowed for by the receiver designer, the ambient temperature for the integrated circuits should not exceed 60°C (stabilised operation) and this will correspond to the maximum permitted chip temperature of 125°C in a limit case. For example, with a cold switch-on from 15°C, and assuming that the room ambient temperature increases during viewing to, say 10degC less than the maximum allowed for, the final ambient temperature for the integrated circuits will reach about 50°C, corresponding to a maximum chip temperature of about 115°C. The chip temperature has risen by about 100degC, 35degC of this caused by the rise in cabinet ambient temperature and 65degC caused by self-heating. The thermal time-constant of a typical chip in a 16-pin envelope is such that its self-heating is almost complete in 90 seconds. A substantial portion of this occurs before the picture tube starts to function. Therefore, for the purpose of calculating from the data the effects of thermal drifts in the integrated circuits, a substantial part of the total increase in chip temperature can be ignored because it occurs during the first minute after switch-on.

Layout requirements

An integrated circuit, owing to the large number of active devices usually contained on the chip, can have a very high power gain between its input and output circuits. In this respect, the layout of the decoder panel is rather more critical than with discrete transistors. Interference between high and low level circuits of different channels can occur unless sufficient attention is given to avoiding common paths and coupling loops in the layout. Experience has shown that, with integrated circuits, a layout following a pattern of earth loops or boxes intended to improve isolation between different circuits is unsatisfactory. A branch pattern for the earthing of the various channels is better. This allows the earth paths for the luminance, chrominance, reference and colour difference signal channels to converge and meet at the RGB output circuit. Individual bypass capacitors of about 100nF should be connected across the supply terminals of the integrated circuits to provide adequate decoupling.

Radiation of harmonics of the 4·43MHz components in the demodulated colour difference signals is minimised by the use of compact filter network components and layout at the outputs of the synchronous demodulators. The contribution to this form of radiation by the RGB output stages is minimised by limiting their frequency response to about 7MHz. However, radiation of the products of demodulation from the picture tube drive signal leads can occur and series resistors connected close to the output transistors are usually found necessary.

A typical recommended layout of the main earth and signal paths is illustrated in schematic form in Fig. 2. Each block includes the appropriate integrated circuit with its peripheral components. The earth point for each block should be as close to the earth pin of the integrated circuit as possible. Note that the chrominance and reference signals do not have common earth paths before detection (by the TBA990), hence crosstalk is minimised. If the necessity for decoupling chokes in the 12V supply circuit is to be avoided, there must similarly be no common paths in the 12V supply lines to the reference and chrominance circuits before the TBA990 demodulator. The earthing of the subcarrier filters between the TBA990 and TBA530 is also arranged to be very close to pin 16 (earth) of the TBA990 to contain the filter currents within the vicinity of the TBA990. Finally, the earth track from the TBA990 is taken to the earth pin of the TBA530 matrix integrated circuit. The luminance and chrominance signals are here combined to form the RGB output signals to the video output stage, and the earthing point of this stage is used as the common earth point for the complete decoder circuit.

The experimental circuit for this decoder was laid out on a printed wiring board measuring 230×170mm.

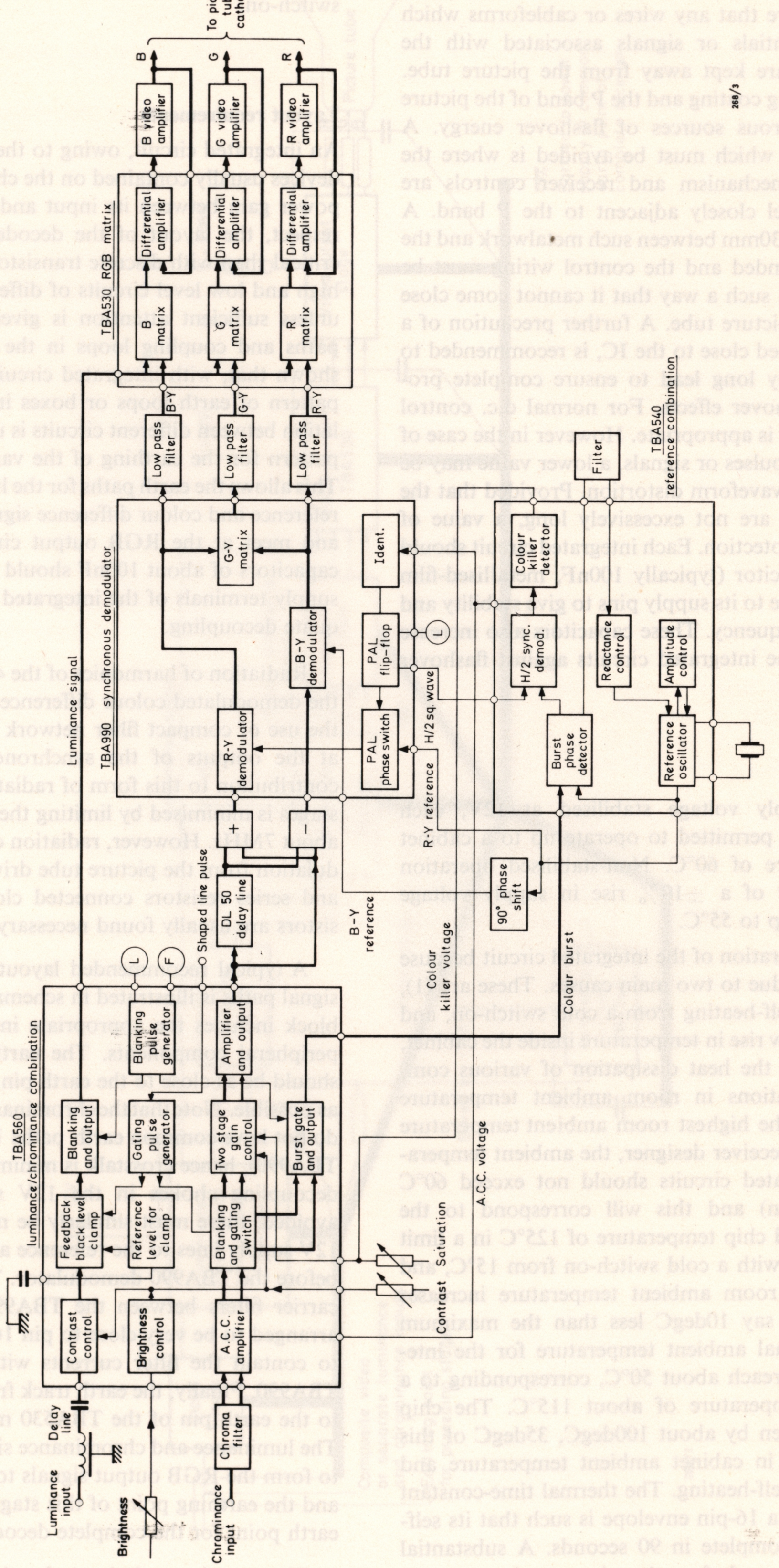
TBA560
luminance/chrominance combination
Luminance input
Delay line
Brightness
Chrominance input
Contrast control
Brightness control
Chroma filter
A.C.C. amplifier
Feedback black level clamp
Reference level for clamp
Blanking and gating switch
Blanking and output
Gating pulse generator
Two stage gain control
Blanking pulse generator
Amplifier and output
Burst gate and output
L
F
Shaped line pulse
Contrast
Saturation
A.C.C. voltage
Colour killer voltage
Colour burst
Luminance signal
TBA990 synchronous demodulator
DL 50 delay line
+
−
R-Y demodulator
B-Y demodulator
B-Y reference
PAL phase switch
PAL flip-flop
Ident.
R-Y reference
H/2 sq. wave
G-Y matrix
90° phase shift
H/2 sync. demod.
Colour killer detector
Burst phase detector
Reactance control
Filter
Reference oscillator
Amplitude control
TBA540
reference combination
Low pass filter
B-Y
G-Y
R-Y
TBA530 RGB matrix
B matrix
G matrix
R matrix
Differential amplifier
B video amplifier
G video amplifier
R video amplifier
B
G
R
To picture tube cathodes
268/3

Fig. 3—Block diagram of decoder system

SYSTEM DESCRIPTION

The colour decoder uses standard PAL processing functions and is shown in the block diagram (Fig. 3). The signal paths, as distinct from control function paths, are shown as bold lines.

In accordance with established UK practice an a.c. coupled and d.c. clamped luminance channel is employed. The input to the decoder may be composite video or separate luminance and chrominance signals (luminance signal amplitude into the TBA560 = 0·5mA black-to-white) and the outputs from the RGB stages are 100V black-to-white amplitude.

The detailed requirements of each integrated circuit in relation to its operation with its peripheral components are described in the published data sheets. The following description deals with the overall operation of the decoder.

DECODER CIRCUIT DESCRIPTION

For the complete circuit diagram and all test references see Fig. 4 (p. 90).

The input circuit of the decoder is arranged to accommodate a composite video input from either an i.f. amplifier equipped with a synchronous demodulator or from a video distribution system. Alternatively, separate luminance and chrominance inputs, for example, from an i.f. amplifier with separate diode detectors, can be used.

The luminance signal can be supplied, for example, from the TCA270 video synchronous demodulator IC. This has a black-to-white amplitude of 1·7V which is applied via a 6MHz sound carrier filter and a delay line terminating resistor R_2 to the luminance delay line ($R_o = 1{\cdot}5k\Omega$). A luminance delay of about 500ns has been found to be the optimum for the complete decoder described, but the actual value required in a particular circuit will depend on such factors as chroma filter bandwidth and the i.f. amplifier response. The total series resistance of about 3kΩ in the luminance signal input level provides the required TBA560 input signal current of 0·5mA black-to-white amplitude.

The chroma trap L_1 C_2 C_3 is designed to give a high rejection at 4·4MHz (20dB) consistent with a narrow 3dB bandwidth (±500kHz) and negligible distortion of the 2T pulse. The luminance signal is a.c. coupled by C_5 into the TBA560. A d.c. bias current of 0·5mA is also fed into pin 3 via R_{10} from the +12V line.

The chroma input to the TBA560 is supplied from the composite video input signal via a chroma filter network. The filter, centred on 4·4MHz, is shown as a black box as its specification depends to a large extent on individual requirements.

The important aspects of chroma bandpass filter design are discussed in the Appendix and two alternative examples are illustrated.

Pulse shaping circuit

A positive-going pulse is required on pin 10 of the TBA560 for the colour-burst gating and black-level clamping functions. This is obtained as follows: a winding on the line output transformer supplies a +18V pulse having a mean level of 0V and this is applied to pin 10 via R_{32} R_{33} D_2 and C_{18}. During the line scan period the charge potential on C_{19} is about 0V. The arrival of a flyback pulse causes D_2 to cease conduction, and the potential across C_{19} rises exponentially as it charges via R_{30} towards +12V. When the trailing edge of the flyback pulse voltage becomes equal to the voltage to which C_{19} has charged, D_2 again conducts and discharges C_{19}, returning its potential to 0V. The instant of conduction of D_2 is determined by the flyback pulse amplitude and is therefore adjustable by R_{33}*. Thus a positive-going sawtooth waveform of 3·5V peak-to-peak amplitude, whose duration is slightly less than that of the flyback pulse, is developed across C_{19}. This waveform is coupled via C_{18} to pin 10 of the TBA560. There is a diode characteristic on this pin so that conduction occurs only during the tip of the sawtooth waveform. The input current to pin 10 operates the luminance clamp and burst gate circuits, so the timing and duration of these functions can be determined by the choice of values for R_{30} C_{19}.

Negative-going pulses for line and field flyback blanking in the luminance channel are required on pin 8. To avoid the need for a second line timebase pulse to the decoder, and also because a positive-going pulse is more readily obtainable from common designs of field timebase, a transistor is employed to develop suitable pulses. TR_1 is non-conducting during the line scan period and saturated for most of the duration of the line flyback pulse because R_{37} has a relatively low value. The network R_{35} R_{36} is arranged to provide the correct amplitude of blanking pulse, which is then coupled to pin 8. The field blanking pulse of 30V peak-to-peak amplitude is applied via R_{38} C_{20} to TR_1. The value of R_{38} is chosen to give a sufficiently long duration of field blanking pulse. In a case where a negative-going field flyback pulse is available, it could, of course, be a.c. coupled directly to pin 8 of the TBA560 but its amplitude must not be greater than 1·5V peak-to-peak. Because TR_1 is saturated for the field flyback period, its output waveform is not suitable for triggering the PAL flip-flop in the TBA990. For this purpose, a positive-going line flyback pulse is directly applied to pin 14 of the TBA990 via R_{29}. Triggering of the PAL flip-flop occurs on the negative-going edge of this pulse.

TBA560 peripheral circuit

The picture brightness is controlled by a variable d.c. potential applied to pin 6 of the TBA560. A variation between 0V and 1·2V will cover the entire range of black level variation (on pin 5) from 0V to 3V. This is more than is needed in practice and the range of the control can be restricted to suit particular requirements.

During the operation of a correctly-adjusted receiver, variations in the transmitted picture can occasionally cause the safe limit of mean beam current (1·5mA total typically) in the picture tube to be exceeded. Such excesses should be dealt with by a reduction in picture contrast to maintain the correct picture black level. A convenient source of beam current information occurs at the earthy end of the e.h.t. supply network. The mean beam current can be sampled directly here and used to control the contrast level in the TBA560. Diode D_1 is forward biased during normal operation by a current of about 1·5mA supplied via the contrast control network R_5 R_6. For all values of mean beam current below 1·5mA, D_1 remains conducting and the contrast control functions normally. Above 1·5mA, however, D_1 becomes non-conducting and the bottom end of the contrast control is driven negatively, thus reducing the contrast level. No threshold level adjustment is required, and provided that the current source for the contrast control network is derived from at least 20V, adequate loop gain is achieved. A BZX70 zener diode is used for D_1 with 10 to 15V reverse breakdown voltage, to limit the negative potential in the event of serious overload and thus protect the IC and the capacitor C_1. The value of C_1 is chosen as a compromise between a small parabolic variation in contrast caused by field frequency ripple in the e.h.t. circuit and an adequately fast reaction time for the control loop. The supply voltage for the contrast control network should be sufficiently ripple-free to avoid the need for further decoupling in the contrast control network, which would make the loop time-constant complicated, possibly introducing oscillatory effects into its operation.

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*The phase performance of the receiver's line flywheel system must be taken into account in determining the nominal phase position of the gating pulse. In a complete receiver having not more than ±0·5μs phase deviation over the working range of the line flywheel system it should be possible to replace R_{33} with a fixed resistor.

A luminance signal of nominally 1·6V black level and 1V black-to-white amplitude is produced on pin 5 and is directly coupled to pin 5 of the TBA530 matrix circuit. The d.c. potentials controlling contrast and saturation are applied independently to pins 2 and 13 respectively. For any given setting of the saturation control R_4 the chroma signal amplitude will track adjustment of the contrast control R_6. Also for any given setting of these controls the contrast and chroma levels track together during operation of the beam current limiting function.

The network R_{15} R_{16} R_{17} sets the d.c. working point of the burst amplifying channel in the TBA560. The a.c.c. potential applied to pin 14 is filtered by the network R_{21} C_{12}. The colour killer potential from pin 7 of the TBA540 is applied via R_{23} to the saturation control point, pin 13 of the TBA560.

The colour burst output from pin 7 of the TBA560 is fed to the TBA540 reference combination via the low pass filter circuit L_2, C_{16} and the coupling capacitor C_{17}. This circuit is included for two main reasons, the principal one being to compensate for residual phase shifts in the decoder. These amount to about 15° lagging with a spread of ±10° so that a leading phase shift of 15° is required from this filter circuit, with an adequate adjustment range. The second requirement of the circuit is to give a voltage gain of about 1·5 since the optimum burst output of the TBA560 is 1V peak-to-peak and the optimum input to the TBA540 is 1·5V peak-to-peak. This can be simply achieved by operating the filter circuit near its reasonant frequency and choosing a suitable Q, which gives a circuit with voltage gain and a reasonably wide adjustment range as required. The circuit has a phase shift at resonance of 90° (lagging) which is simply compensated for by a suitable choice of output connections from pins 4 and 6 of the TBA540; these are as shown in the main circuit diagram (Fig. 4).

TBA540 peripheral circuit

The TBA540 reference oscillator IC receives its colour burst input signal on pin 5 at an amplitude of 1·5V peak-to-peak (under a.c.c. control). The a.p.c. loop phase detector loads and filter are connected to pins 13 and 14. A crystal of 20pF nominal load capacitance is connected between pins 1 and 15 to form the reference oscillator. The oscillator reference output waveform from pin 4 is applied to transformer L_3 which produces an antiphase waveform on pin 6. These waveforms are applied via the 90° phase shifting network R_{24} C_{27} and via d.c. blocking capacitors C_{37} C_{48} to pins 2 and 8 of the TBA990 demodulator circuit at an amplitude of about 700mV peak-to-peak.

A synchronously generated a.c.c. potential is produced at pin 9 and is fed via resistor R_{21} to the TBA560. With no burst signal input to the TBA540 the potential on pin 9 (TP8) is set by R_{50} to +4V. When the burst signal is applied and if the PAL flip-flop phase in the TBA990 is correct, this potential will drop until a.c.c. control is established (1·5V peak-to-peak burst signal amplitude). This condition corresponds to about +1V on pin 9 of the TBA540. If the flip-flop phase is incorrect the potential on pin 9 would rise to +10V, passing a positive potential to the flip-flop ident control point, pin 1 of the TBA990. The PAL flip-flop in the TBA990 would stop, thus removing the switching waveform from the a.c.c. synchronous detector in the TBA540 (pin 8). As a result the a.c.c. potential on pin 9 would drop towards 0V thus allowing the flip-flop to start up again. The colour killer switching output from the TBA540 is produced at pin 7 from the collector of a transistor which is saturated for incorrect ident (giving a voltage of +250mV) and is off for correct ident; the switching of this transistor occurs as the voltage on pin 9 passes +2·5V.

TBA990 peripheral circuit

The TBA990 synchronous demodulator IC receives its chrominance input signals on pins 10 and 13 from the PAL delay line (type DL50). The reference subcarrier signals from the TBA540 are received on pins 2 and 8. No adjustment is required to set the 90° phase-shifted reference signal to pin 2. The tolerance in the phase-shift, allowing for the effect of the input inpedance of pin 2, is less than ±5° providing that the tolerance for C_{27} is ±2% (such as the Mullard C333 series) and for R is ±5%.

The demodulated colour difference signals are supplied at pins 4, 5, and 7 and their d.c. levels are adjusted by potentiometers R_{56} R_{59} R_{60}. These outputs must be filtered by R_{65} C_{41} C_{42} etc., to reduce the residual 4·43MHz and 8·86MHz carrier components present. The h.f. currents in the filter capacitors must be confined to the immediate vicinity of the TBA990 to prevent leakage into the wideband TBA530 and video output stage circuits. Otherwise, radiation of harmonics of these frequencies from the video stages could enter the tuner or i.f. stages of the receiver and produce objectionable patterning on the picture.

Two alternative filter arrangements are suitable depending on allowable levels of subcarrier patterning on the picture. With the filter networks shown in Fig. 4 a 3dB bandwidth of 1MHz is obtained with an attenuation at 4·4MHz of 16dB. The resulting 4·4MHz component of the signal at the cathodes of the picture tube is then typically 2V peak-to-peak. An amplitude of 4V peak-to-peak is regarded as the limit to avoid objectionable patterning. The attenuation at 8·8MHz and above is sufficiently large if the filter capacitors are returned directly to the earth connection of the TBA990. The performance of this type of filter is probably adequate for receivers having a high performance specification.

A single-stage type of filter can be employed, however, having a single capacitor from each TBA990 output terminal to earth and a direct connection to eachTBA530 input terminal. A value of 56pF is suitable. This will give a −3dB bandwidth of 900 kHz and an attenuation at 4·4MHz of 13dB resulting in a 4·4MHz component of the signal at the cathodes of the picture tube of about 3V peak-to-peak. However, the response of such a filter is very dependent upon the tolerance in the output resistance of the TBA990 and this may result in a spread in amplitude up to 4V peak-to-peak. Thus this type of filter is more suitable for small-screen receivers.

TBA530 peripheral circuit

The TBA530 IC provides the matrixing of the colour difference signals with the luminance signal together with a very high internal gain between the inputs and the outputs. This enables a large amount of feedback to be employed over each video output stage thus stabilising their signal gains and d.c. levels against voltage, temperature, and ageing effects.

The three high voltage transistor output stages are similar to each other, therefore only one, the Red (TR_2), will be described. Operation is from a 205V stabilised supply, reduced to a basic 173V by the potential divider network R_{75} R_{77} R_{78}. The voltage gain, with negative feedback, between the colour difference input pins 2, 3 and 4 of the TBA530 and the collectors of the output transistors is nominally 100.

The black level potential at the collector of TR_2 is nominally +140V for raster cut-off and is determined by three factors:

1) the black level setting of the luminance signal applied to pin 5 of the TBA530 (nominally +1·6V),
2) the d.c. level setting of the (R-Y) signal applied to pin 4 of the TBA530 (this is adjusted by the potential from R_{60} connected to pin 12 of the TBA990), and
3) the ratio of the potential divider resistors R_{75} R_{77}. The potential produced at the junction of these resistors is used for the d.c. feedback.

If the d.c. levels of the signals are correctly set, a black level of +140V at the collector of TR_2 will result in about +6V at the junction of R_{75} R_{77}. This equals the potential at the junction of resistors R_{68} R_{70} connected to the +12V supply. The potential at the slider of R_{73} will thus feed a potential of +6V to the feedback terminal of the TBA530, pin 9. If the black level of the signal at the collector of the output transistor changes because of supply voltage variations, temperature drifts etc., the feedback circuit adjusts the d.c. potential applied from pin 10 to the base of TR_2 so that the correct black level is maintained. The potentiometer R_{73} adjusts the signal feedback so that the overall output stage gain can be varied to set up the picture tube drive signal amplitudes. The purpose of the constant black level bridge network R_{68} R_{70} R_{73} R_{75} R_{77} already described is to enable this to be done without shifting the black levels of the output signals. Adjustable potentiometers are necessary on only two of the output stages. H.F. compensation of each video amplifier is obtained by partial decoupling of the emitter resistor by C_{50}, R_{72} being included to limit the gain of the stage at very high frequencies thus removing any peaks in the response around 20MHz. The frequency response compensation of the complete circuit is achieved in the feedback loop by means of C_{49} R_{69} C_{51} R_{76}.

ALIGNMENT PROCEDURE

The alignment procedure is described below in some detail for clarity. Many of the procedures are intended to give a simple indication suitable for a production test.

1) Check that the l.t. supply lies within 12V±5% or set it to this level in the case of an adjustable regulation.

Luminance channel adjustments

2) Connect TP1 to earth to kill the chroma channel, so that the output signals from the TBA990 are zero amplitude.
3) Connect a d.c. voltage of 1·6V to pin 5 of the TBA530, by disconnecting the link between TP9 and TP10 and connecting TP9 to TP11. The voltage obtained from the potential divider R_{62} R_{64} is the nominal black level for the luminance input signal to the TBA530 and should correspond to picture tube raster cut-off.
4) Connect a voltmeter between TP18 and TP19.
5) Adjust R_{56}, which adjusts the d.c. level of the colour difference output signals of the TBA990, until the voltage between TP18 and TP19 is reduced to zero. This establishes the correct voltage at the collector of the BF336 video output transistor TR_4 and also at the cathode of the blue gun of the CRT, to be nominal black level (raster cut-off). Thus, the bridge network formed by R_{94} R_{96} R_{101} R_{102} is balanced.
6) Adjust R_{59} and R_{60}, which independently adjust the d.c. levels of the G-Y and R-Y outputs of the TBA990, to similarly obtain zero voltage between TP16 and TP17 and between TP14 and TP15 respectively.

7) The cut-off controls used to adjust the voltages applied to the a_1 electrodes of the CRT are now adjusted for raster cut-off on each gun.

8) Disconnect the link between TP9 and TP11 and reconnect TP9 to TP10. Apply a "grey scale" signal from a pattern generator and adjust the contrast and brightness controls to obtain a suitable picture.

9) Adjust variable resistors R_{73} and R_{84} to obtain the correct white point of the display. As the voltage across the arms of the bridge in each video output stage has already been adjusted to zero at black level, this adjustment can usually be carried out without having to readjust the cut-off (a_1) controls. In a few cases, variations in CRT drive characteristics between guns will make a small readjustment of cut-off controls necessary to ensure a uniform grey scale.

10) L_1 should be adjusted to minimise the residual subcarrier content in the video drive to pin 5 of the TBA530, by observing the luminance signal at TP10 when a colour bar signal, for example, is applied from a pattern generator.

Chrominance channel adjustments

11) The following adjustments to the chrominance circuits should be carried out with a colour bar signal from a pattern generator. Adjust the chrominance bandpass filter at the input of the decoder for optimum response. Remove the short-circuit between TP1 and earth, and remove the link between TP1 and TP2. Adjust the saturation control to give a suitable picture on the screen.

With the flywheel system correctly phased, check that the gating pulse for the colour burst is correctly timed by observing the gated burst at TP7. Adjust the timing of the burst gating pulse by means of R_{33} if necessary. The burst should be centrally situated in the gating interval.

12) Adjust the reference oscillator TBA540 as follows: Short circuit TP5 to TP6 in order to disable the burst phase detector. The starting point of the a.c.c. voltage (corresponding to reception of zero chrominance signal) can now be adjusted by observing the voltage at TP8. This should be set to 4·0V by means of R_{50}.

13) The reference oscillator frequency may be adjusted by means of C_{23} until the rolling of the colours is almost brought to a standstill; that is, the regenerated subcarrier frequency is within a few hertz of the transmitted subcarrier frequency.

14) Remove the short circuit between TP5 and TP6. The reference oscillator should lock to the colour burst.

15) Adjust the a.c.c. gain control R_{52} until the burst amplitude at TP7 is 1·5V peak-to-peak.

16) The adjustment of subcarrier phase and delay line balance can be achieved either by the use of a pattern generator such as the Philips PM5508 or by the use of a standard colour bar signal and an oscilloscope as described in procedures 17 to 22.

With the PM5508 pattern generator, the adjustment procedure is as follows. Select the PHASE pattern and adjust the coil L_2 until the colour of each bar is the same in both parts of the screen. Select the DELAY pattern and adjust R_{53} and L_4 until the "Hanover bars" visible are reduced to zero. Adjustments of the delay line input and output coils L_4 and L_5 both affect the phase delay. However, the output coil should be pre-adjusted during manufacture to its nominal inductance of 8·9μH, and delay (phase balance) adjustments are made with the input coil L_4, which has twice the effect of the output coil L_5 on the delay. By this means most of the delay spreads can be adjusted out within the permitted −19 to +36% variation of input coil inductance, without any serious reduction of the frequency response of the delayed signal path. If the worst-case spreads of delay are encountered, so that it is not possible to achieve phase balance with the input coil L_4, then the output coil L_5 may be adjusted. The total variation possible with −19 to +36% inductance range in both coils is sufficient to take up all spreads with minimum reduction of the frequency response, the bandwidth remaining greater than 1·8MHz.

After adjustment of the delay line phase and amplitude balance, select the PHASE pattern again and check the subcarrier phase adjustment.

17) The alternative procedure, with a standard colour bar signal and an oscilloscope, is as follows: the oscilloscope is connected to TP12 (R-Y colour difference output of the TBA990) and triggered by line pulses in such a way that two adjacent lines are superimposed.

18) Open circuit TP3 and TP4. This effectively isolates the delay line and transforms the decoder to simple PAL operation, which makes subcarrier phase errors obvious as line-to-line differences. To correct the phase of the R-Y subcarrier the burst phase shift coil L_2 is adjusted until the double pictures seen on the oscilloscope are made to coincide.

19) Connect the oscilloscope to TP13 and check that the line-by-line difference in the B-Y output of the TBA990 (at TP13) is reduced to zero, or nearly so. Thus the phase adjustment of the reference subcarriers is made by a null method, which gives a very clear indication of error.

20) The phase adjustment of the DL50 delay line can now be carried out. Replace the connection between TP3 and TP4, and continue to observe the B-Y colour difference output at TP13 or the R-Y output at TP12. Errors in phase balance of the delay line will be seen as line-by-line differences in the colour bars with large R-Y content, namely the cyan, green, magenta, and red bars. The phase adjustment should be performed as in procedure 16; that is, beginning with the delay line input coil L_4, until the double pictures viewed on the oscilloscope are made to coincide.

21) Amplitude balance errors in the delay line, which will result in the presence of B-Y chrominance signal in the R-Y chrominance input to the TBA990 and vice versa, will not give rise to any line-by-line disturbances in the colour difference outputs, as the phases of the reference subcarrier signals have been precisely adjusted in procedures 18 and 19. To obtain a line-by-line error which will indicate any amplitude unbalance of the delay line it is thus necessary to shift the overall phase of the reference subcarrier signals from the nominal position, preferably by 90°. Connect a 1nF capacitor across L_2 and C_{17} which will give a phase error greater than 30° and adjust R_{53} to reduce the line-by-line differences to zero, viewing the B-Y signal at TP13 or the R-Y signal at TP12, as before.

22) Remove the 1nF shorting capacitor and reconnect the link between TP1 and TP2 to restore correct operation of the colour killer.

This completes the alignment of the decoder, with a choice of techniques from which the one more suitable for a production test can be chosen.

TABLE 1

Coil winding details

Coil number	Former	Winding	Turns	Wire	Core
L_1	EIH P1011/1	Wavewound 6·4mm length	70	0·1mm en. cu.	4×0·5×6/500
L_2	EIH P1011/1	Wavewound 6·4mm length	70	0·1mm en. cu.	4×0·5×6/500
L_3	NEOSID 4060 (F14)	Scramble	18+18	0·1mm en. cu. bifilar wire	NEOSID 4060
L_A	EIH P1011/1	Single layer	40+40 bifilar	0·1mm en. cu.	NEOSID 500×6mm
L_B	EIH P1011/1	Single layer	20+20 bifilar	0·1mm en. cu.	NEOSID 500×6mm
L_C	EIH P1011/1	Wavewound 6·4mm length	80	0·1mm en. cu.	NEOSID 500×6mm

L_4 and L_5 are standard Mullard coils AT4044/00 and AT4044/01 respectively.

COMPONENTS

Resistors

The Mullard CR25 series can be used for all resistors except those in the following positions:

R_{15}, R_{16}, R_{17}, R_{25}, R_{27}, R_{43} and R_{44}—MR25 series.

R_{39}, R_{78}, R_{91}, R_{104}—Vitrohm 6W 214–1 series.

R_{75}, R_{89} and R_{102}—Vitrohm 2W 210–1 series.

R_{79}, R_{80}, R_{92}, R_{93}, R_{105}, R_{106} and R_{107} Dubilier BTA (carbon) series, 1W.

Adjustable Resistors

Variable resistors

R_4, R_6 and R_{12}—Morganite 30N series.

Preset resistors

R_{33}, R_{50}, R_{52}, R_{53}, R_{56}, R_{59}, R_{60}, R_{73} and R_{84}—Radiospares miniature presets.

Capacitors

Circuit No.	Value	Type No.
C_1	100μF 25V	016 16101
C_2	47pF	C333CC/C47E
C_3	47pF	C333CC/C47E
C_4	100nF	C280AE/P100K
C_5	68μF 16V	016 15689
C_6	47nF	C280AE/P47K
C_7	47nF	C280AE/P47K
C_8	100nF	C280AE/P100K
C_9	100nF	C280AE/P100K
C_{10}	10μF 25V	015 16109
C_{11}	100nF	C280AE/P100K
C_{12}	1·5μF 63V	015 90001
C_{14}	68μF 16V	016 15689
C_{15}	10μF 25V	015 16109
C_{16}	33pF	C333CC/C33E
C_{17}	220pF	C333CH/C220E
C_{18}	470pF	
C_{19}	6·8nF	
C_{20}	100nF	C280AE/P100K
C_{21}	100nF	C280AE/P100K
C_{22}	100nF	C280AE/P100K
C_{23}	4 to 60pF	808 01011
C_{24}	18pF	C333CB/C18E
C_{25}	82pF	C333CC/C82E
C_{26}	22pF	C333CC/C22E
C_{27}	33pF	C333CC/C33E
C_{28}	100nF	C280AE/P100K
C_{29}	15μF 40V	015 17159
C_{30}	330nF	C280AE/A330K

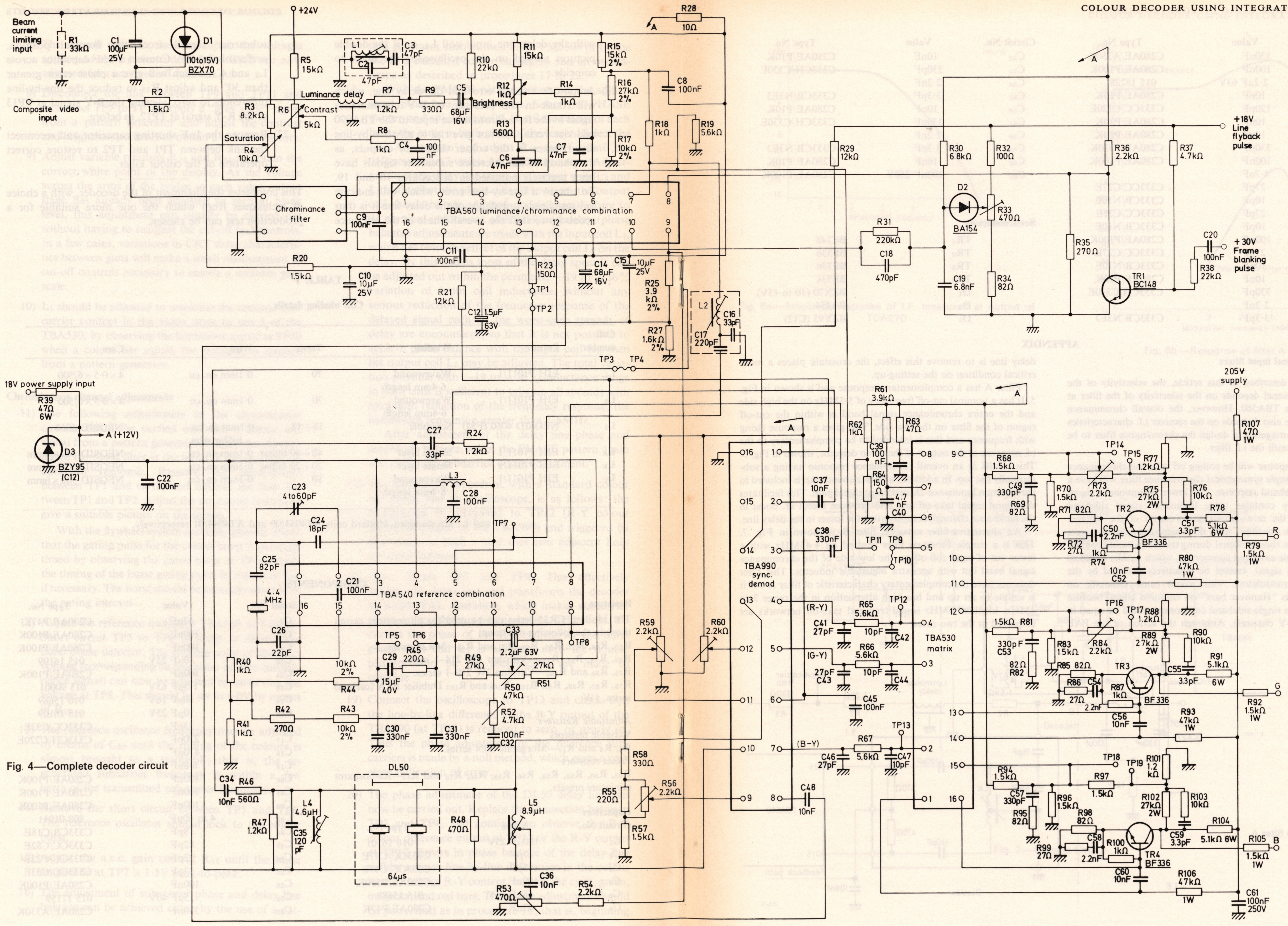
Beam current limiting input
Composite video input
+24V
R1 33kΩ
C1 100μF 25V
D1 (10to15V) BZX70
R2 1.5kΩ
R3 8.2kΩ
Saturation
R4 10kΩ
R6 Contrast 5kΩ
R5 15kΩ
L1
C2 47pF
C3 47pF
Luminance delay
R7 1.2kΩ
R9 330Ω
C5 68μF 16V
R8 1kΩ
C4 100nF
R10 22kΩ
R11 15kΩ
R12 1kΩ Brightness
R13 560Ω
C6 47nF
C7 47nF
R14 1kΩ
R15 15kΩ 2%
R16 27kΩ 2%
R17 10kΩ 2%
R28 10Ω
C8 100nF
R18 1kΩ
R19 5.6kΩ
Chrominance filter
C9 100nF
TBA560 luminance/chrominance combination
R20 1.5kΩ
C10 10μF 25V
C11 100nF
R21 12kΩ
C12 1.5μF 63V
R23 150Ω
TP1
TP2
C14 68μF 16V
C15 10μF 25V
R25 3.9kΩ 2%
R27 1.6kΩ 2%
L2
C16 33pF
C17 220pF
TP3
TP4
18V power supply input
R39 47Ω 6W
A (+12V)
D3 BZY95 (C12)
C22 100nF
C27 33pF
R24 1.2kΩ
L3
C28 100nF
C23 4 to 60pF
C24 18pF
TP7
C25 82pF
4.4 MHz
C21 100nF
C26 22pF
TBA540 reference combination
TP5
TP6
C29 15μF 40V
R45 220Ω
C33 2.2μF 63V
R49 27kΩ
R51 27kΩ
TP8
R40 1kΩ
R44 10kΩ 2%
R50 47kΩ
R42 270Ω
R43 10kΩ 2%
R52 4.7kΩ
C32 100nF
R41 1kΩ
C30 330nF
C31 330nF
R59 2.2kΩ
R60 2.2kΩ
R58 330Ω
R55 220Ω
R56 2.2kΩ
R57 1.5kΩ
C34 10nF
R46 560Ω
DL50
64μs
L4 4.6μH
C35 120pF
R47 1.2kΩ
R48 470Ω
L5 8.9μH
C36 10nF
R53 470Ω
R54 2.2kΩ
R29 12kΩ
R30 6.8kΩ
R32 100Ω
D2 BA154
R33 470Ω
R31 220kΩ
C18 470pF
C19 6.8nF
R34 82Ω
R35 270Ω
R36 2.2kΩ
R37 4.7kΩ
+18V Line flyback pulse
C20 100nF
+30V Frame blanking pulse
R38 22kΩ
TR1 BC148
R61 3.9kΩ
R62 1kΩ
R63 47Ω
C39 100nF
R64 150Ω
C40 4.7nF
C37 10nF
C38 330nF
TP11
TP9
TP10
TBA990 sync. demod
(R-Y)
(G-Y)
(B-Y)
R65 5.6kΩ
C41 27pF
C42 10pF
R66 5.6kΩ
C43 27pF
C44 10pF
C45 100nF
TP12
TP13
R67 5.6kΩ
C46 27pF
C47 10pF
C48 10nF
TBA530 matrix
205V supply
R107 47Ω 1W
TP14
TP15
R68 1.5kΩ
C49 330pF
R69 82Ω
R70 1.5kΩ
R73 2.2kΩ
R77 1.2kΩ
R75 27kΩ 2W
R76 10kΩ
R71 82Ω
C50 2.2nF
TR2 BF336
C51 3.3pF
R78 5.1kΩ 6W
R
R72 27Ω
R74 1kΩ
R79 1.5kΩ 1W
R80 47kΩ 1W
C52 10nF
TP16
TP17
R88 1.2kΩ
R81 1.5kΩ
C53 330pF
R82 82Ω
R83 1.5kΩ
R84 2.2kΩ
R89 27kΩ 2W
R90 10kΩ
R85 82Ω
C55 3.3pF
R91 5.1kΩ 6W
TR3 BF336
R86 27Ω
C54 2.2nF
R87 1kΩ
G
R92 1.5kΩ 1W
R93 47kΩ 1W
C56 10nF
TP18
TP19
R101 1.2kΩ
R94 1.5kΩ
R97 1.5kΩ
C57 330pF
R95 82Ω
R96 1.5kΩ
R98 82Ω
R102 27kΩ 2W
R103 10kΩ
C59 3.3pF
R104 5.1kΩ 6W
B
R105 1.5kΩ 1W
R99 27Ω
C58 2.2nF
R100 1kΩ
TR4 BF336
C60 10nF
R106 47kΩ 1W
C61 100nF 250V
A

Fig. 4—Complete decoder circuit

Circuit No.	Value	Type No.
C_{31}	330nF	C280AE/A330K
C_{32}	100nF	C280AE/P100K
C_{33}	2·2μF 63V	015 18228
C_{34}	10nF	C280AE/P10K
C_{35}	120pF	C333CC/C120E
C_{36}	10nF	C280AE/P10K
C_{37}	10nF	C280AE/P10K
C_{38}	330nF	C280AE/P330K
C_{39}	100nF	C280AE/P100K
C_{40}	4·7nF	
C_{41}	27pF	C333CC/C27E
C_{42}	10pF	C333CB/N10E
C_{43}	27pF	C333CC/C27E
C_{44}	10pF	C333CB/N10E
C_{45}	100nF	C280AE/P100K
C_{46}	27pF	C333CC/C27E
C_{47}	10pF	C333CB/N10E
C_{48}	10nF	C280AE/P10K
C_{49}	330pF	C333CH/C330E
C_{50}	2·2nF	
C_{51}	3·3pF	C333CB/N3E3

Circuit No.	Value	Type No.
C_{52}	10nF	C280AE/P10K
C_{53}	330pF	C333CH/C330E
C_{54}	2·2nF	
C_{55}	3·3pF	C333CB/N3E3
C_{56}	10nF	C280AE/P10K
C_{57}	330pF	C333CH/C330E
C_{58}	2·2nF	
C_{59}	3·3pF	C333CB/N3E3
C_{60}	10nF	C280AE/P10K
C_{61}	100nF 250V	C280AE/P100K

Semiconductors

TR_1	BC148
TR_2	BF336
TR_3	BF336
TR_4	BF336
D_1	BZX70 (10 to 15V)
D_2	BA154
D_3	BZY95 (C12)

APPENDIX

Chrominance signal input filters

In the decoder described in this article, the selectivity of the chrominance channel depends on the selectivity of the filter at the input to the TBA560. However, the overall chrominance channel response also depends on the receiver i.f. characteristics so that it is advantageous to design the chrominance filter to be complementary with the i.f. filter.

As the i.f. response will be rolling off over the chrominance signal band, a simple symmetrical chrominance filter will have a larger lower sideband response. The lower chrominance signal sideband usually contains more luminance signal sideband energy so that the cross-colour performance of the receiver would suffer with this filter. Also, if the sideband responses were very unequal, the chroma signal during transients would contain a significant single-sideband component, which, unlike the ideal double-sideband signal, cannot be selectively detected by the synchronous demodulators. This would cause crosstalk on transients, that is "Hanover bars" on coloured edges, because the output of the single-sideband component would be equal in the R-Y and B-Y channels. Although the action of the PAL delay line is to remove this effect, the crosstalk places a more critical condition on the setting-up.

Filter A has a complementary response and is shown in Fig. 5. It has a nominal cut-off frequency of 5·5MHz on the high side and the entire chrominance signal band is within the cut-off region of the filter on the low side. This gives a response rising with frequency and this is intended to be complementary to the i.f. response at the output of the video detector, shown in Fig. 6. This results in an overall chrominance response having a substantially flat top. In addition, a 6MHz sound trap is included in the common luminance-chrominance signal path. This facilitates the sound signal take-off and also provides useful i.f. boost in the luminance channel, compensating for losses in the delay line.

An alternative filter network, filter B, is shown in Fig. 7. This is a simple bandpass filter centred on 4·43MHz with a faster out-of-band roll-off on the low side of the chrominance signal band but with an extra adjustable inductor. This filter does not have the complementary characteristic of filter A but it is simple to set up and has high attenuation in the range 2 to 3MHz. Identical 6MHz sound trap and take-off networks are employed in the two cases.

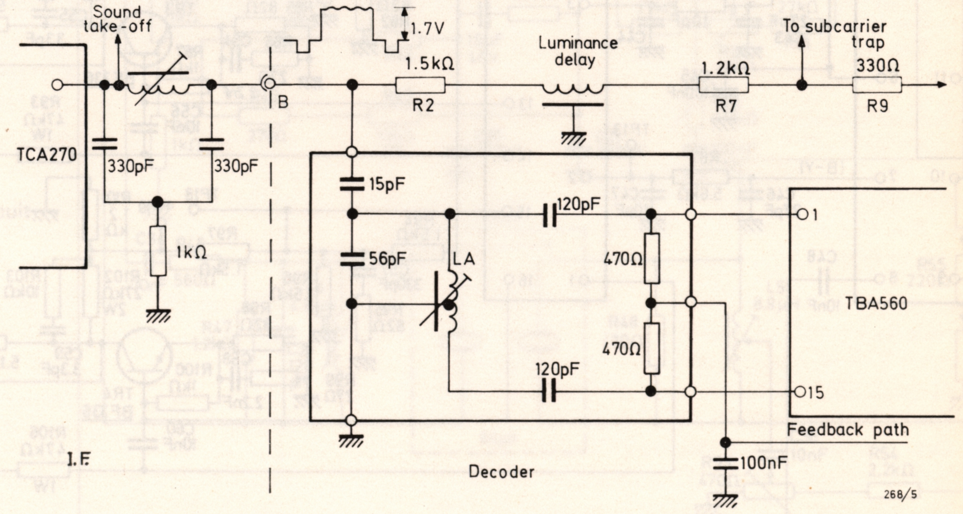

Fig. 5—Chroma filter A

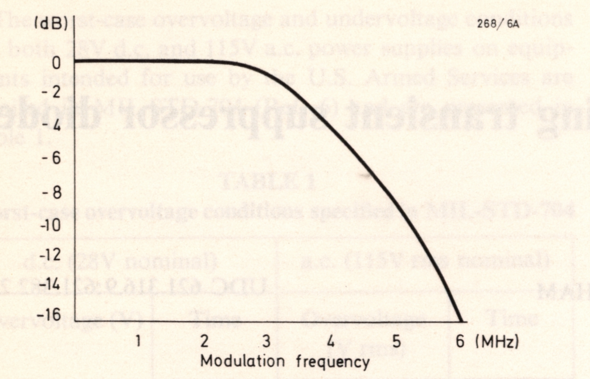

Fig. 6a—Amplitude response of I.F. measured at output of TCA270

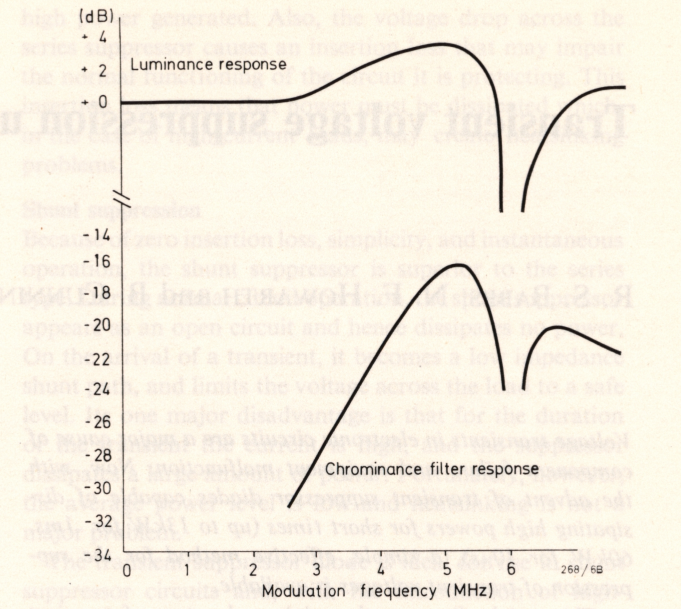

Fig. 6b—Response of filter A

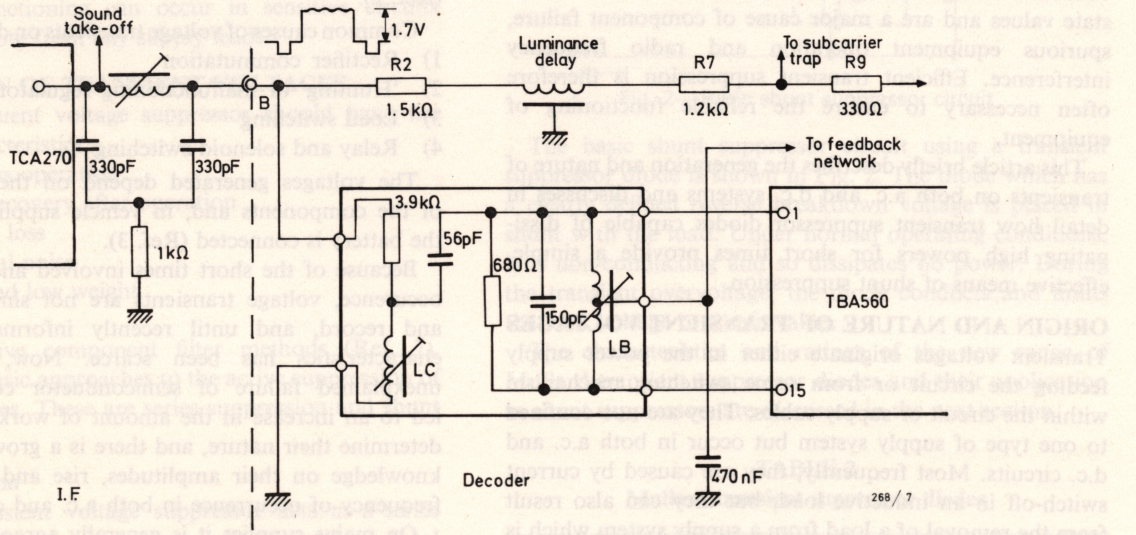

Fig. 7—Chroma filter B

Transient voltage suppression using transient suppressor diodes

R. S. BABBS, N. F. HOWARTH and B. CUNNINGHAM

UDC 621.316.9:621.382.232

Voltage transients in electronic circuits are a major cause of component failure and equipment malfunction. Now, with the advent of transient suppressor diodes capable of dissipating high powers for short times (up to 13kW for 1ms, 60kW for 10μs), a simple, effective method for the suppression of transient voltages is available.

This article discusses the origin and nature of transient voltages and considers the advantages and disadvantages of shunt and series suppression. Information on the characteristics of the transient suppressor diode is given and various practical shunt circuits are described. Finally, curves are presented which enable the user to choose a diode which gives the desired suppression and allows safe dissipation of the transient energy.

INTRODUCTION

Transient voltages in electronic systems far exceed steady-state values and are a major cause of component failure, spurious equipment operation and radio frequency interference. Efficient transient suppression is therefore often necessary to ensure the reliable functioning of equipment.

This article briefly describes the generation and nature of transients on both a.c. and d.c. systems and discusses in detail how transient suppressor diodes capable of dissipating high powers for short times provide a simple, effective means of shunt suppression.

ORIGIN AND NATURE OF TRANSIENT VOLTAGES

Transient voltages originate either in the power supply feeding the circuit or from some switching mechanism within the circuit or supply cables. They are not confined to one type of supply system but occur in both a.c. and d.c. circuits. Most frequently, they are caused by current switch-off in an inductive load, but they can also result from the removal of a load from a supply system which is common to a number of units.

In an a.c. rectifier circuit using a transformer and choke input filter, shown in Fig. 1, some common causes of transient voltages are:

1) Energisation of the transformer primary
2) De-energisation of the transformer primary
3) Removal of the load
4) Rectifier commutation
5) Transients from the a.c. supply to the transformer primary.

The voltages generated by the first four items depend on the component values (Ref. 1). The last depends on the characteristics of the a.c. supply impedance, the loads connected to the system and the devices which switch these loads. Of these, the a.c. supply impedance at the supply frequency is necessarily low for good regulation, and it is the impedance of the supply at low radio frequencies which determines the amplitudes of the transient voltages (Ref. 2).

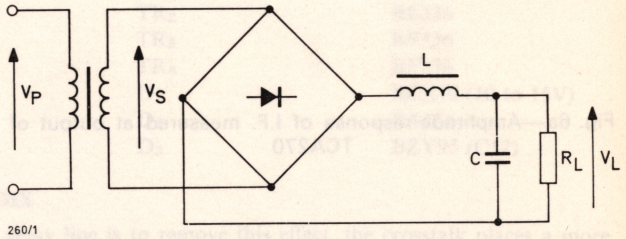

Fig. 1—Rectifier circuit with transformer and choke input filter

Common causes of voltage transients on d.c. supplies are:

1) Rectifier commutation
2) 'Hunting' or malfunctioning regulators
3) Load switching
4) Relay and solenoid switching

The voltages generated depend on the characteristics of the components and, in vehicle supplies, on whether the battery is connected (Ref. 3).

Because of the short times involved and their random occurence, voltage transients are not simple to observe and record, and until recently information on their characteristics has been scarce. Now, however, the unexplained failure of semiconductor components has led to an increase in the amount of work being done to determine their nature, and there is a growing amount of knowledge on their amplitudes, rise and fall times and frequency of occurrence in both a.c. and d.c. systems.

On mains supplies it is generally agreed that the total voltage between line and neutral can at times reach as high as 1kV, of which the transient voltage is at least 650V. In some industrial premises, 400V spikes occur on an average twice a day and 200V spikes, as many as 500 times a day (Refs. 2 and 4).

On d.c. systems, particularly those in vehicles, the switching of relays and solenoids causes voltages in excess of 1kV on 28V coils (Ref. 5). Load switching can cause 100 to 120V spikes lasting for as long as 50ms.

Authors: R. S. Babbs of Mullard Central Application Laboratory and N. F. Howarth and B. Cunningham of Mullard, Stockport.

The worst-case overvoltage and undervoltage conditions for both 28V d.c. and 115V a.c. power supplies on equipments intended for use by the U.S. Armed Services are detailed in MIL-STD-704 (Ref. 6) and are presented in Table 1.

TABLE 1
Worst-case overvoltage conditions specified in MIL-STD-704

d.c. (28V nominal)		a.c. (115V rms nominal)	
Overvoltage (V)	Time	Overvoltage (V rms)	Time
80	40ms	190	100ms
76	80ms	184	200ms
68	113ms	174	400ms
44	400ms	155	1s
38	880ms	139	3s
36	5s	137	5s

These values represent the permissible maxima on equipment supplies, and equipments should function reliably when operating from supplies with such limits. Suppression may be necessary depending on the equipments and the circuits they contain.

EFFECTS OF TRANSIENT VOLTAGES

The effects of transient voltages can be divided into two broad classifications: damage to components and malfunctioning of equipment. Damage is generally confined to those components directly connected to the supply, whereas malfunctioning can occur in sensitive circuits apparently remote from any supply leads.

SUPPRESSION OF TRANSIENT VOLTAGES

The ideal transient voltage suppressor should have the following characteristics:

1) Instantaneous operation
2) Immediate recovery after operation
3) No insertion loss
4) No additional noise
5) Small size and low weight
6) Low cost

Besides passive component filter methods (Ref. 7), there are two basic approaches to the active suppression of transient voltages. These are series suppression and shunt suppression.

Series suppression

The series transient voltage suppressor acts as a series impedance which varies from a low resistance under normal operating conditions to a very high resistance when a voltage transient occurs. In one typical method, a transistor is placed in series with the load and biased so that, under normal operating conditions, it is in saturation. When a transient voltage appears, the transistor comes out of saturation (it may possibly cut off), its resistance is increased, and the voltage across the load is limited to a safe level.

There are several disadvantages to series suppression. The suppressor must be able to withstand the transient voltage, and, if it does not turn off, be able to dissipate the high power generated. Also, the voltage drop across the series suppressor causes an insertion loss that may impair the normal functioning of the circuit it is protecting. This insertion loss means that power must be dissipated which, in the case of high current loads, may create heatsinking problems.

Shunt suppression

Because of zero insertion loss, simplicity, and instantaneous operation, the shunt suppressor is superior to the series type. During normal circuit operation, the shunt suppressor appears as an open circuit and hence dissipates no power. On the arrival of a transient, it becomes a low impedance shunt path, and limits the voltage across the load to a safe level. Its one major disadvantage is that for the duration of the transient the current is high, and the suppressor dissipates a large amount of power. Fortunately, however, the average power level is low and heatsinking is not a major problem.

The transient suppressor diode is ideal for use in shunt suppressor circuits and, with the introduction of high-power devices such as the BZW86, the suppression of transients up to 13kW for 1ms, or 30kW for 100μs, is now possible.

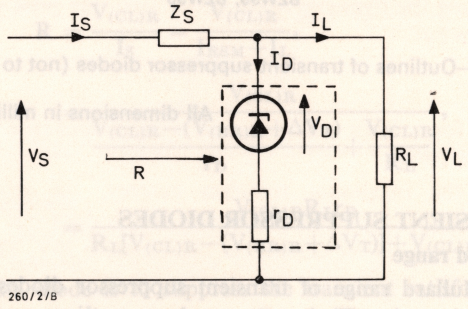

Fig. 2—Basic shunt suppressor circuit

The basic shunt suppressor circuit using a transient suppressor diode is shown in Fig. 2. The diode which has a clearly defined reverse breakdown voltage is placed in shunt with the load. Under normal operating conditions, it is non-conducting and so dissipates no power. During the transient overvoltage, the diode conducts and limits the load voltage to a safe value.

The characteristics and ratings of the new range of Mullard transient suppressor diodes and their application as shunt suppressors are discussed in the next section.

TABLE 2
Mullard transient suppressor diodes

Series number	Suffix	Pulse power rating (t_p = 1ms)*	Outlines	
			VASCA	JEDEC
BZW96	3V9 to 7V5	110W	SO-16	DO-1
BZW70	5V6 to 62	400W	SO-15	
BZW95	5V6 to 62	400W	SO-16	DO-1
BZW93	5V6 to 62	400W	SO-10	DO-4
BZW91	5V6 to 62	5kW	SO-13	DO-5
BZW86	7V5 to 62	13kW	SO-29A	DO-30

*Non-repetitive, rectangular pulses, T_j=25°C before pulse

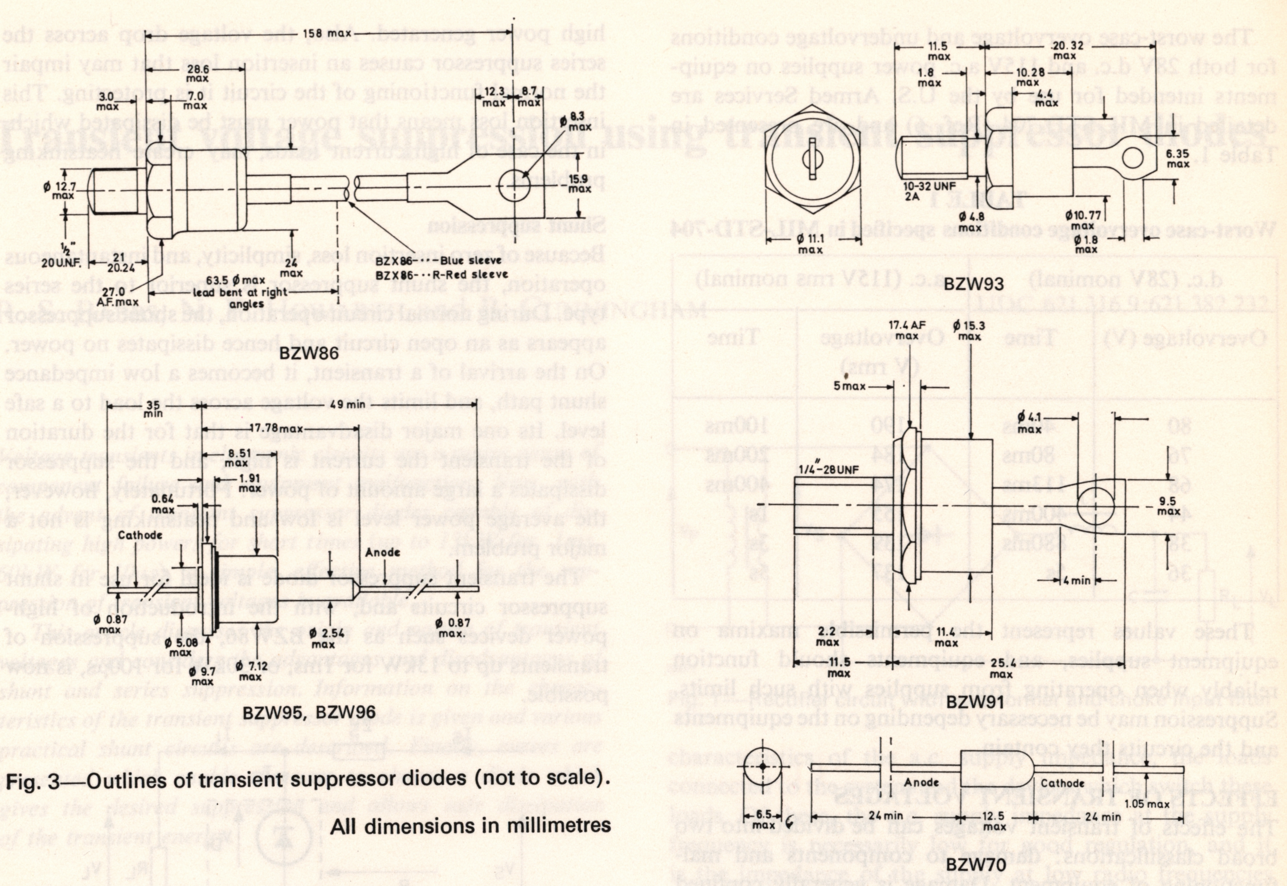

Fig. 3—Outlines of transient suppressor diodes (not to scale).

All dimensions in millimetres

TRANSIENT SUPPRESSOR DIODES

Mullard range

The Mullard range of transient suppressor diodes comprises six series. Their type numbers, outlines and non-repetitive pulse power ratings for a pulse duration of 1ms are given in Table 2, and dimensioned outlines are shown in Fig. 3.

The suffix to the type number does not include a tolerance letter but indicates the 'stand-off' voltage of the device. Reverse polarity versions (stud mounted to anode) of the BZW93, BZW91 and BZW86 are indicated by the suffix 'R', for example, BZW91-36R.

Definitions

The current-voltage characteristic of the transient suppressor diode is shown in Fig. 4. The forward curve is of the normal diode form but in the reverse direction the characteristic exhibits a sharp knee at the breakdown voltage $V_{(BR)R}$. The voltage 10% below the minimum value of the breakdown voltage ($V_{(BR)R}$min) is called the 'stand-off' voltage (V_R). It is defined as the reverse voltage at which the leakage current does not exceed the maximum value quoted in the published data.

For a given supply voltage, it is necessary to choose a suppressor diode whose stand-off voltage is equal to or greater than the highest normal supply voltage. Under such conditions, the diode passes only the leakage current and the power dissipated is negligibly small. After breakdown, the diode reverse current rises rapidly. For a large increase in reverse current (to I_{RSM}) the diode voltage increases to the 'clamping voltage' $V_{(CL)R}$, which is generally less than $2V_R$. The dissipation in the diode is then $V_{(CL)R}I_{RSM}$ and the diode should be chosen so that this dissipation is within the maximum rating. This point is considered further in a later section.

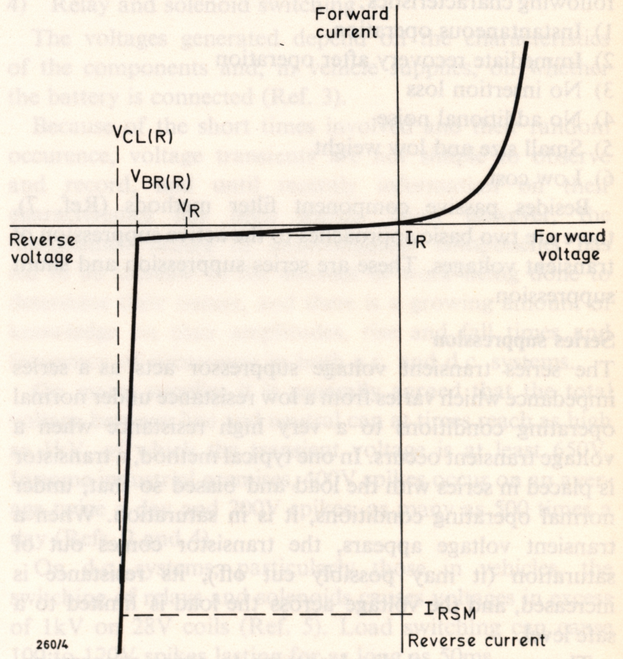

Fig. 4—Current-voltage characteristic of transient suppressor diode

Characteristics and ratings

Clamping voltage against transient current

The clamping voltage of a suppressor diode depends on both the transient current through the diode and its duration.

Figs. 12 to 23 present curves of peak non-repetitive reverse current as a function of clamping voltage for a number of rectangular and step-and-exponential-decay (Fig. 5) pulse durations. For ease of reference, these curves, together with the transient power ratings described in the next section, are grouped separately on pages 100 to 107. At a given maximum current, the curves show the maximum voltage across the diode. For example, for the BZW91-11 (Fig. 21a) at $I_{RSM} = 100A$, $V_{(CL)R}$ rises to 17·8V after 10μs, 18·5V after 100μs and 21·2V after 1ms. Because the dissipation is $V_{(CL)R}I_{RSM}$, the maximum permissible current decreases as the pulse duration increases.

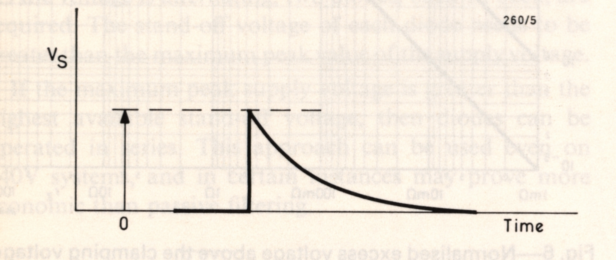

Fig. 5—Step-and-exponential-decay transient waveform

If I_{RSM}max is known, the curves in Figs. 12 to 23 enable the designer to determine directly the clamping voltage for any transient duration. Intermediate curves can be derived by extrapolation from the starting points shown on the $V_{(CL)R}$max axis.

Transient power ratings

Generally, transients occur at random and, compared with their duration, the period between them is long. Hence the duty ratio is very low and, in the majority of cases, operation corresponds to non-repetitive conditions.

Figs. 24 to 29 relate P_{RSM}max to pulse duration for a range of junction temperatures prior to the pulse. The solid and broken curves are for rectangular and step-and-exponential-decay pulses respectively.

OPERATION OF THE TRANSIENT SUPPRESSOR DIODE

The clamping voltage is given by the three terms of the following equation:

$$V_{(CL)R} = V_{(BR)R}+I_{RSM}r_D+P_{RSM}V_{(BR)R}\,Z_{th(t)}\,S_R/100,$$

where

$V_{(BR)R}$ is the reverse breakdown voltage,

I_{RSM} is the diode current during the transient,

r_D is the dynamic resistance of the diode,

P_{RSM} is the power dissipated in the diode,

$Z_{th(t)}$ is the transient thermal impedance from junction to ambient,

S_R is the temperature coefficient of the diode in %/deg C.

The last term in the equation is the change of voltage (ΔV_T) caused by the change in temperature of the junction during the transient. It is positive or negative depending on the sign of the temperature coefficient which itself depends on the diode breakdown voltage. It is negative for diodes with $V_{(BR)R}$ below about 5·6V and positive for diodes above this voltage.

The maximum non-repetitive rectangular pulse power ratings are derived assuming that the junction temperature reaches its maximum permissible transient value at the end of the pulse. Thus, for a diode with a given breakdown voltage, and hence S_R, ΔV_T is almost independent of pulse duration.

Hence, in Fig. 2, during the transient:

$$V_{(CL)R} = V_{(BR)R}+\Delta V_T+I_{RSM}r_D.$$

(Diode capacitance can be ignored)

Therefore,

$$I_{RSM} = \frac{V_{(CL)R}-(V_{(BR)R}+\Delta V_T)}{r_D}$$

But

$$I_L = V_{(CL)R}/R_L,$$

and

$$I_S = I_{RSM}+I_L.$$

Therefore, the equivalent resistance (R in Fig. 2) is:

$$R = \frac{V_{(CL)R}}{I_S} = \frac{V_{(CL)R}}{I_{RSM}+I_L},$$

$$= \frac{V_{(CL)R}}{\dfrac{V_{(CL)R}-(V_{(BR)R}+\Delta V_T)}{r_D}+\dfrac{V_{(CL)R}}{R_L}},$$

$$= \frac{V_{(CL)R}R_Lr_D}{R_L[V_{(CL)R}-(V_{(BR)R}+\Delta V_T)]+V_{(CL)R}r_D}.$$

If the diode is to suppress the transient satisfactorily,

$$r_D \ll R_L.$$

Therefore,

$$R \simeq \frac{V_{(CL)R}}{V_{(CL)R}-(V_{(BR)R}+\Delta V_T)}.r_D.$$

But

$$V_{(CL)R} = I_SR,$$

$$= \frac{V_S-V_{(CL)R}}{Z_S}.R,$$

$$= \frac{V_S-V_{(CL)R}}{Z_S}.\frac{V_{(CL)R}}{V_{(CL)R}-(V_{(BR)R}+\Delta V_T)}.r_D.$$

During the transient, the supply voltage is much higher than the load voltage; that is:

$$V_S \gg V_{(CL)R}.$$

Therefore,

$$V_{(CL)R} = \frac{V_S}{Z_S}.\frac{V_{(CL)R}}{V_{(CL)R}-(V_{(BR)R}+\Delta V_T)}.r_D.$$

Dividing by $V_{(CL)R}$ gives:

$$1 = \frac{V_S}{Z_S}.\frac{1}{V_{(CL)R}-(V_{(BR)R}+\Delta V_T)}.r_D.$$

Therefore,

$$Z_S[V_{(CL)R}-(V_{(BR)R}+\Delta V_T)] = V_Sr_D,$$

or

$$V_{(CL)R} = V_{(BR)R}+\Delta V_T+\frac{r_D}{Z_S}.V_S.$$

This simple approach shows that for good suppression the dynamic resistance of the diode needs to be small compared with the impedance of the supply. Transient suppressor diodes are designed to have this necessary low dynamic resistance (see, for example, Fig. 21a for the BZW91-11 at $t_p = 10\mu s$ where $r_D = 5m\Omega$).

CHOICE OF DIODE AND ITS RESULTANT PERFORMANCE

One method of choosing the correct diode is illustrated by the following examples.

Example 1: Supply impedance known

Consider a 12V±5% supply. Suppose measurements indicate that:

transient amplitude (step-and-exponential-decay)	= 200V
transient duration	= 100μs
total supply impedance	= 1Ω.

Under normal operating conditions, the diode must not conduct, hence a diode with a 13V stand-off voltage is required. During the transient, the diode conducts and, assuming the dynamic resistance is zero, the peak current is given by:

$$I_{RSM} = \frac{V_S}{Z_S}.$$

Thus, for a 200V transient and a line impedance of 1Ω, I_{RSM} is 200A.

At the maximum transient current, the maximum clamping voltage of a suppressor diode does not exceed twice the stand-off voltage, in this example 26V. Thus the maximum transient power dissipation is:

$$P_{RSM}\text{max} = 5{\cdot}2\text{kW}.$$

The dashed curves in Fig. 28 show that the BZW91-13 will safely dissipate this power for the known transient duration (100μs).

Checking against Fig. 20a it is seen that $V_{(CL)R}$max at I_{RSM} = 200A is 22·5V. This gives a revised value for P_{RSM}max of 4·5kW and confirms that the BZW91-13 is a suitable diode for the system.

If the transients are known to be squarewave in form, the same procedure as that outlined above can be followed except that the full-line curves in Figs. 24 to 29 and the appropriate squarewave curves in Figs. 12 to 23 must be used.

Example 2: Supply impedance unknown

If the supply impedance is not known, it is necessary to measure or estimate the supply *inductance*.

Consider a 12·6Vnom (16Vmax) system. Suppose measurements indicate that:

transient amplitude (step-and-exponential-decay)	= 200V,
transient duration	= 100μs,
total supply inductance	= 100μH.

Under normal operating conditions the diode must not conduct. Its stand-off voltage (V_R) must therefore be the maximum normal supply voltage, in this case 16V.

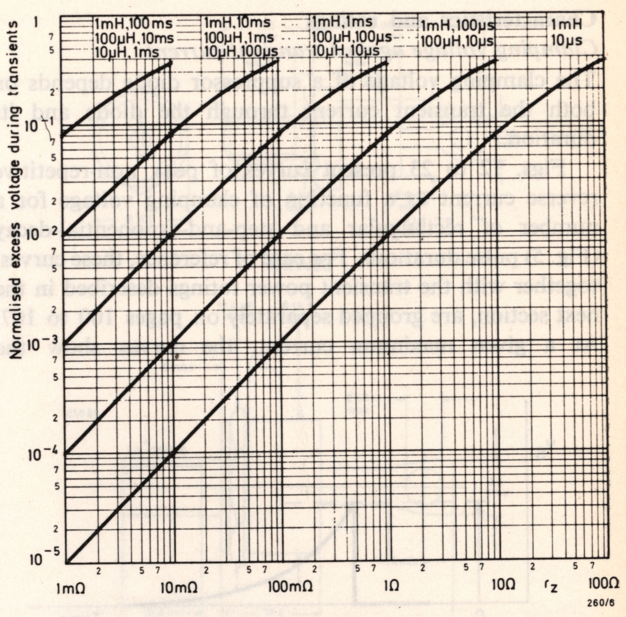

Fig. 6—Normalised excess voltage above the clamping voltage as a function of dynamic impedance for various values of line inductance and transient duration

Measured values of dynamic resistance (r_D) for all diode types operating at their maximum current ratings lie in the range 5 to 200mΩ. As a starting point, therefore, it is reasonable to assume a value for r_D of 50mΩ.

Fig. 6 shows maximum normalised excess voltage across the diode plotted against r_D for various combinations of total supply inductance and transient duration (see Appendix for derivation). In the present example, for r_D = 50mΩ and transient duration = 100μs, Fig. 6 shows that the normalised excess voltage (N.E.V.) is:

$$\text{N.E.V.} = 4{\cdot}4\times10^{-2}\text{V/V}.$$

As the measured transient amplitude is 200V, the excess voltage is:

$$V_{Excess} = 8{\cdot}8\text{V}.$$

Thus, as a first estimate:

$$I_{RSM} = V_{Excess}/r_D = 8{\cdot}8/50\times10^{-3} = 175\text{A}.$$

For diodes with maximum current ratings above this value, $V_{(CL)R}$max is about 2×V_R, in this instance 32V.

Therefore,

$$P_{RSM}\text{max} = V_{(CL)R}\text{max}\ I_{RSM} = 5{\cdot}25\text{kW}.$$

Fig. 28 shows that the BZW91-16 will safely dissipate this power for the known transient duration (100μs).

Now, Fig. 20b shows that for the BZW91-16, $V_{(CL)R}$ max at I_{RSM} = 175A is 27V and a revised value for r_D is about 10mΩ. Repetition of the procedure outlined above using this new value of r_D gives:

N.E.V. $= 1\times10^{-2}$V/V
V_{Excess} = 2V
I_{RSM} = 200A
$V_{(CL)R}$max = 27V
P_{RSM}max = 5·4kW.

These figures confirm that the BZW91-16 is a suitable diode for the system.

It should be noted that if a lower clamping voltage at a given current is required, a larger diode can be used. Also, if P_{RSM} is found to be above the maximum ratings of the largest diode, additional supply inductance is required.

APPLICATIONS OF TRANSIENT SUPPRESSOR DIODES

A.C. Supplies

A circuit for suppressing transient voltages on a.c. supplies using transient suppressor diodes is given in Fig. 7. As the voltage is alternating, two diodes, back-to-back, are required. The stand-off voltage of each diode needs to be greater than the maximum peak value of the supply voltage.

If the maximum peak supply voltage is greater than the highest available stand-off voltage, then diodes can be operated in series. This approach can be used even on 240V systems, and in certain instances may prove more economic than passive filtering.

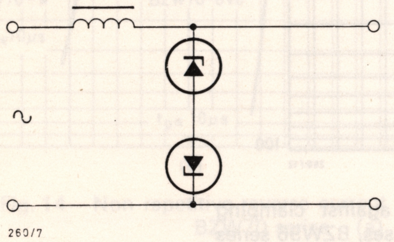

Fig. 7—Suppression of transients on a.c. supplies

Transformer

Fig. 8 shows how transient suppressor diodes are used to suppress voltages generated by the energising and de-energising of a transformer primary. Two back-to-back diodes are used. The source impedance in this instance is the mains impedance plus the resistance and leakage reactance of the transformer.

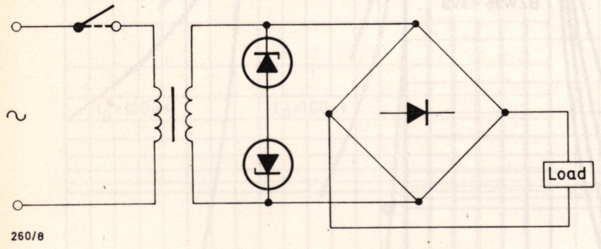

Fig. 8—Suppression of transients caused by the energisation and de-energisation of a transformer primary

Load switching

Fig. 9 shows the position of a suppressor diode for protection against transient voltages caused by load switching.

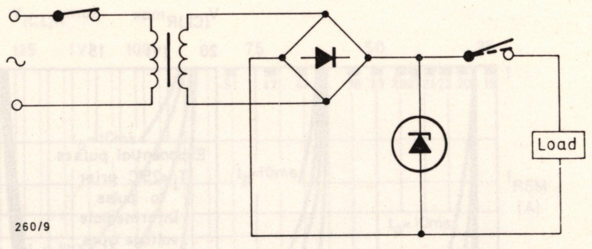

Fig. 9—Suppression of transients caused by load switching

Load short-circuiting

Fig. 10 shows a circuit protected from lengthy short-circuiting of the load by circuit breakers which necessarily have inductive windings. Shorting the load can cause a transient voltage of more than twice the normal supply voltage, until the circuit breaker opens. A transient suppressor diode across the load protects the system.

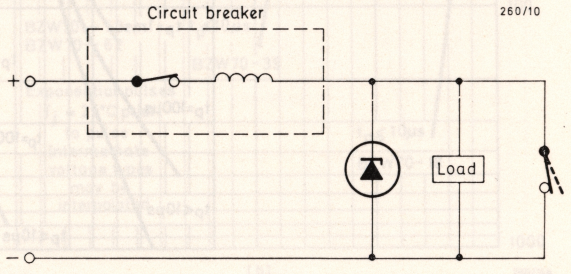

Fig. 10—Suppression of transients caused by load shorting

Line transients

Fig. 11 illustrates the simplicity of line surge suppression with a transient suppressor diode. The necessary series impedance is generally provided by the inductance of the supply leads.

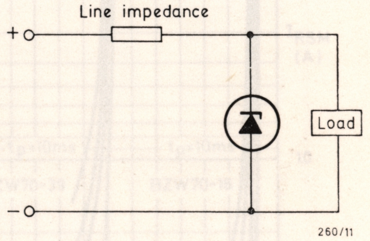

Fig. 11—Protection against line transients

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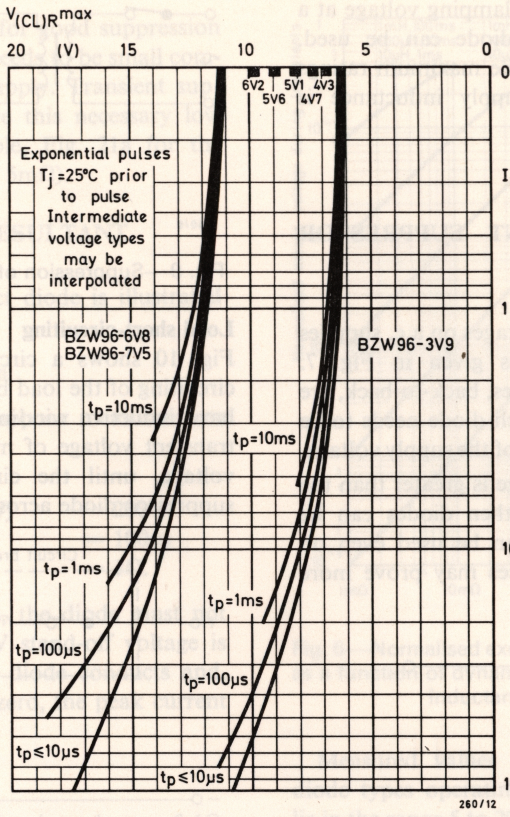

Fig. 12—Non-repetitive reverse current against clamping voltage for step-and-exponential-decay pulses, BZW96 series

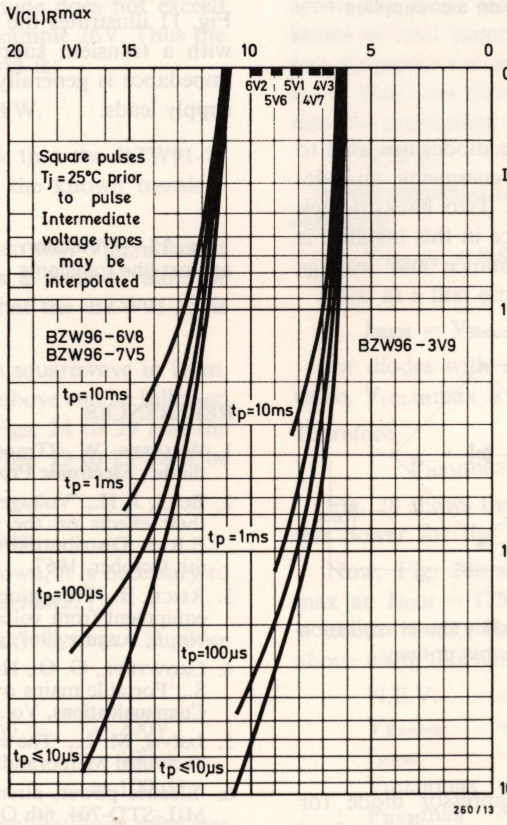

Fig. 13—Non-repetitive reverse current against clamping voltage for squarewave pulses, BZW96 series

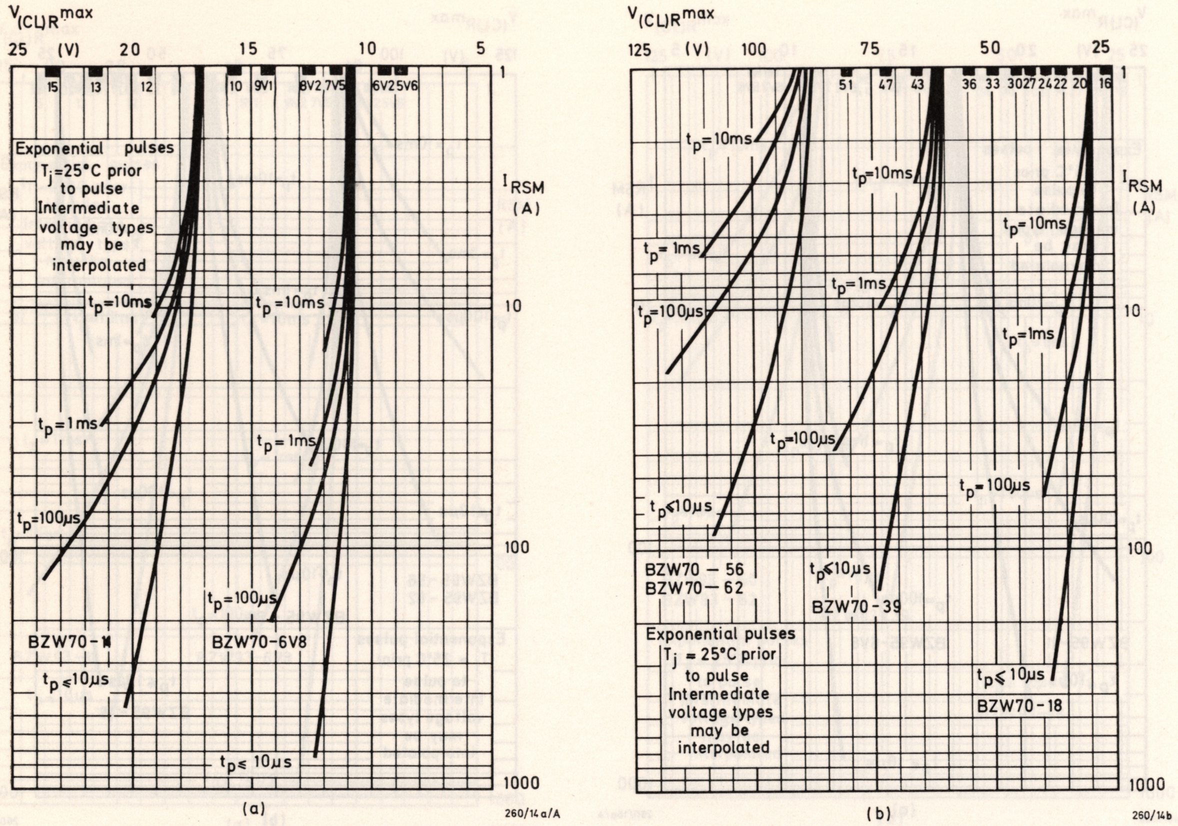

Fig. 14—Non-repetitive reverse current against clamping voltage for step-and-exponential-decay pulses, BZW70 series (a) $V_{(CL)R}$ = 5 to 25V (b) $V_{(CL)R}$ = 25 to 125V

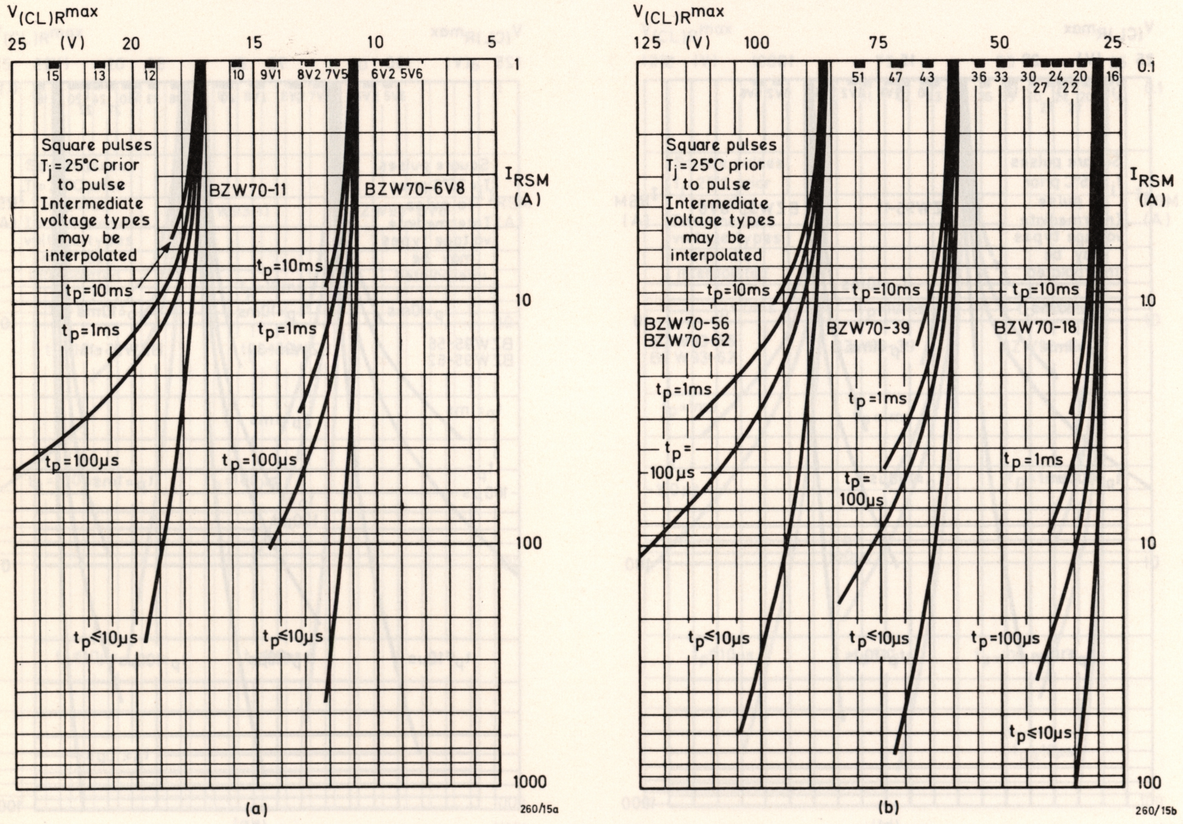

Fig. 15—Non-repetitive reverse current against clamping voltage for squarewave pulses, BZW70 series (a) $V_{(CL)R}$ = 5 to 25V (b) $V_{(CL)R}$ = 25 to 125V

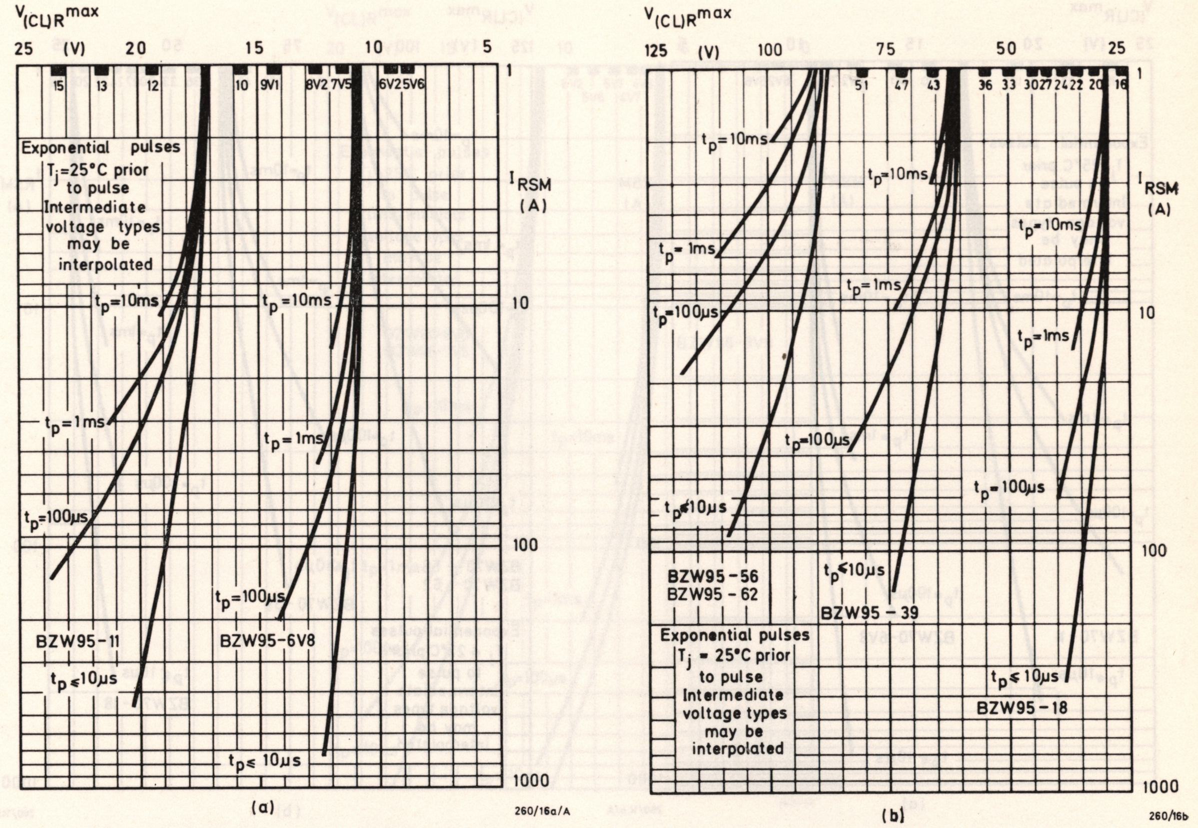

Fig. 16—Non-repetitive reverse current against clamping voltage for step-and-exponential-decay pulses, BZW95 series (a) $V_{(CL)R} = 5$ to 25V (b) $V_{(CL)R} = 25$ to 125V

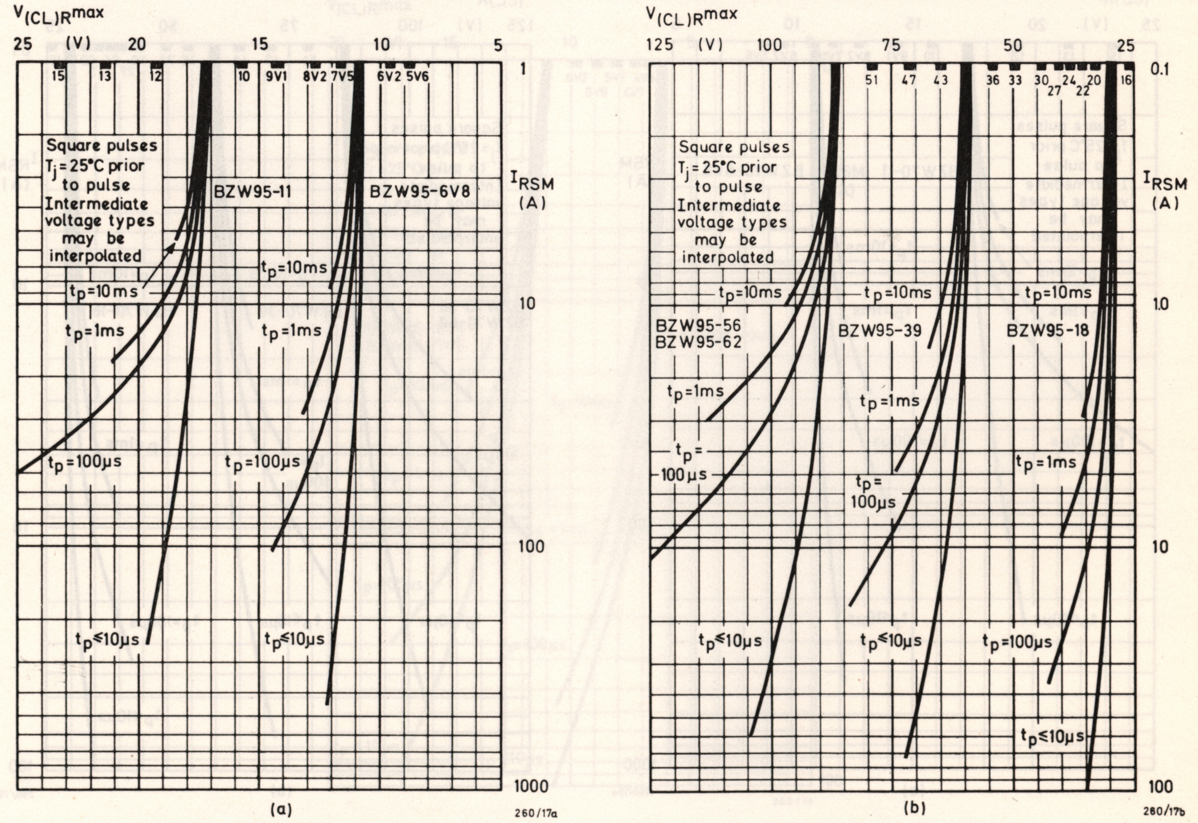

Fig. 17—Non-repetitive reverse current against clamping voltage for squarewave pulses, BZW95 series (a) $V_{(CL)R} = 5$ to 25V (b) $V_{(CL)R} = 25$ to 125V

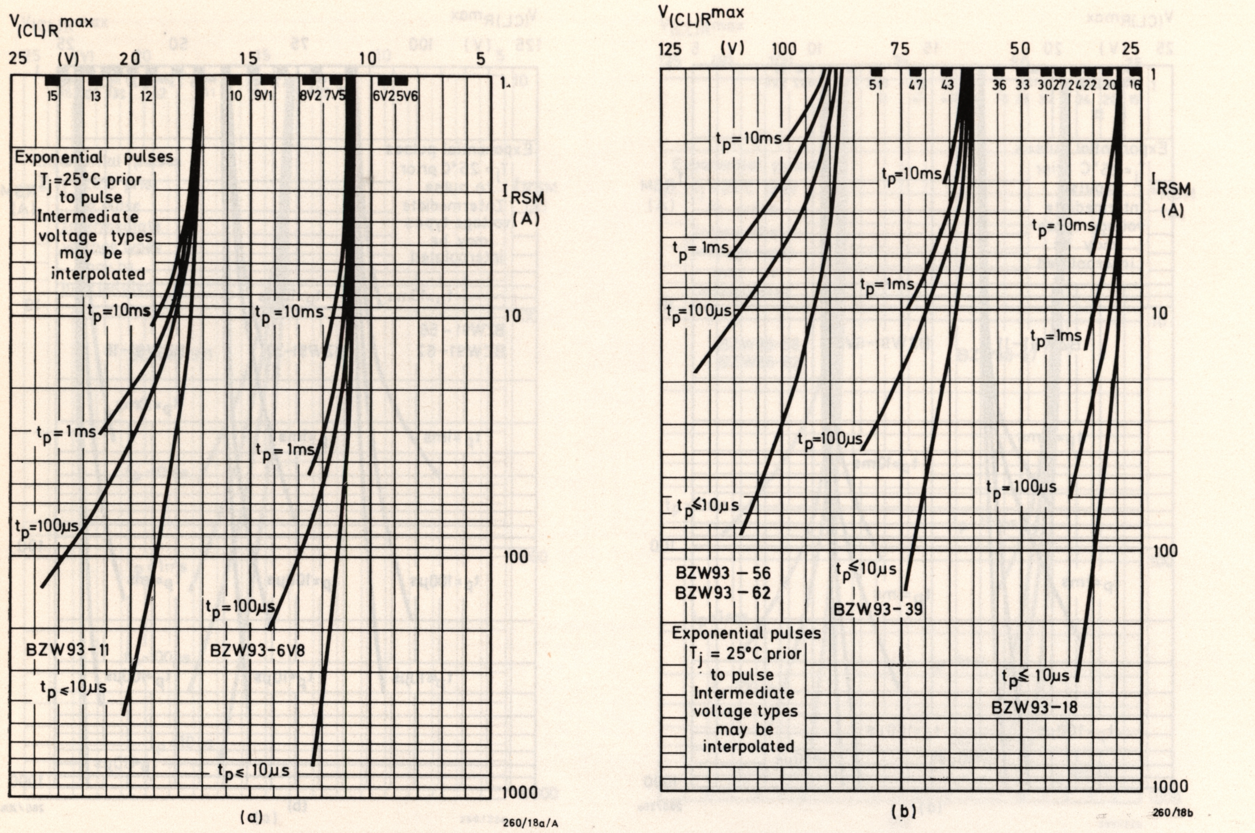

Fig. 18—Non-repetitive reverse current against clamping voltage for step-and-exponential-decay pulses, BZW93 series (a) $V_{(CL)R} = 5$ to 25V (b) $V_{(CL)R} = 25$ to 125V

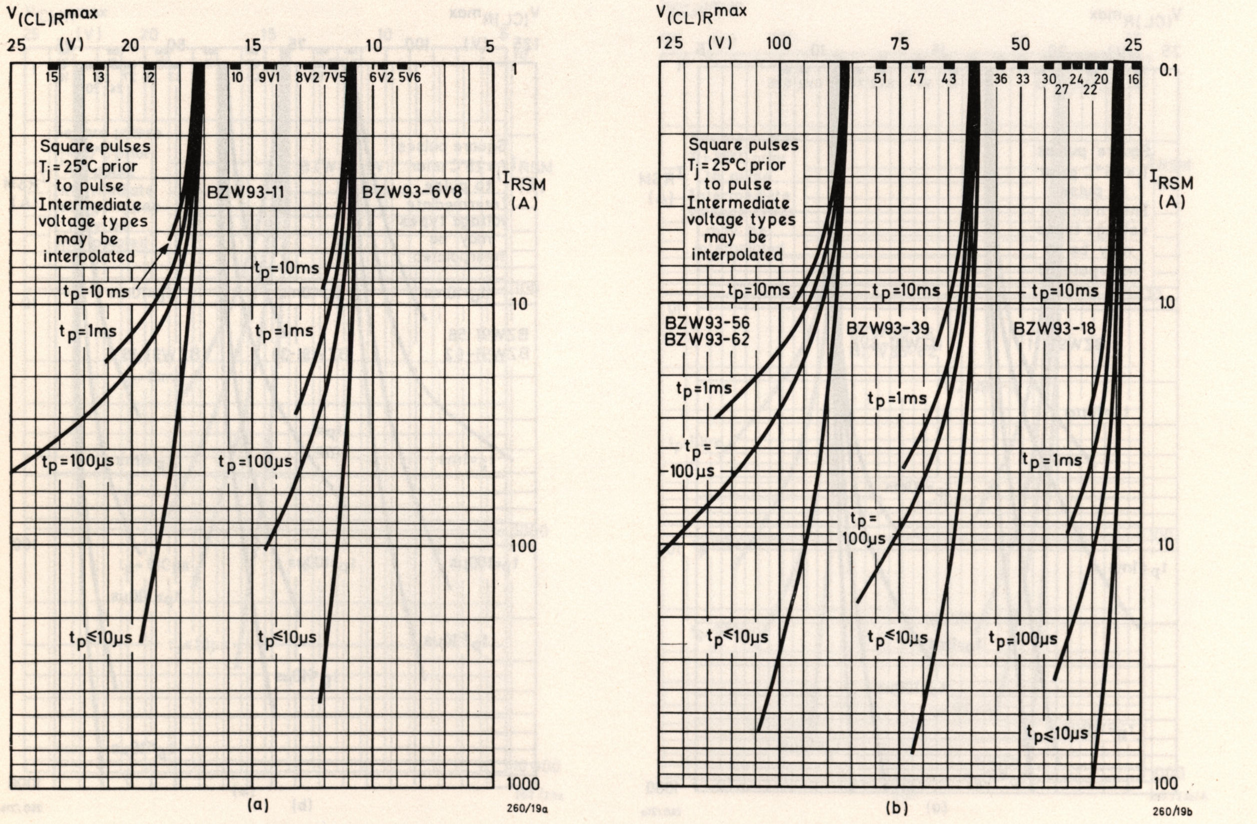

Fig. 19—Non-repetitive reverse current against clamping voltage for squarewave pulses, BZW93 series (a) $V_{(CL)R} = 5$ to 25V (b) $V_{(CL)R} = 25$ to 125V

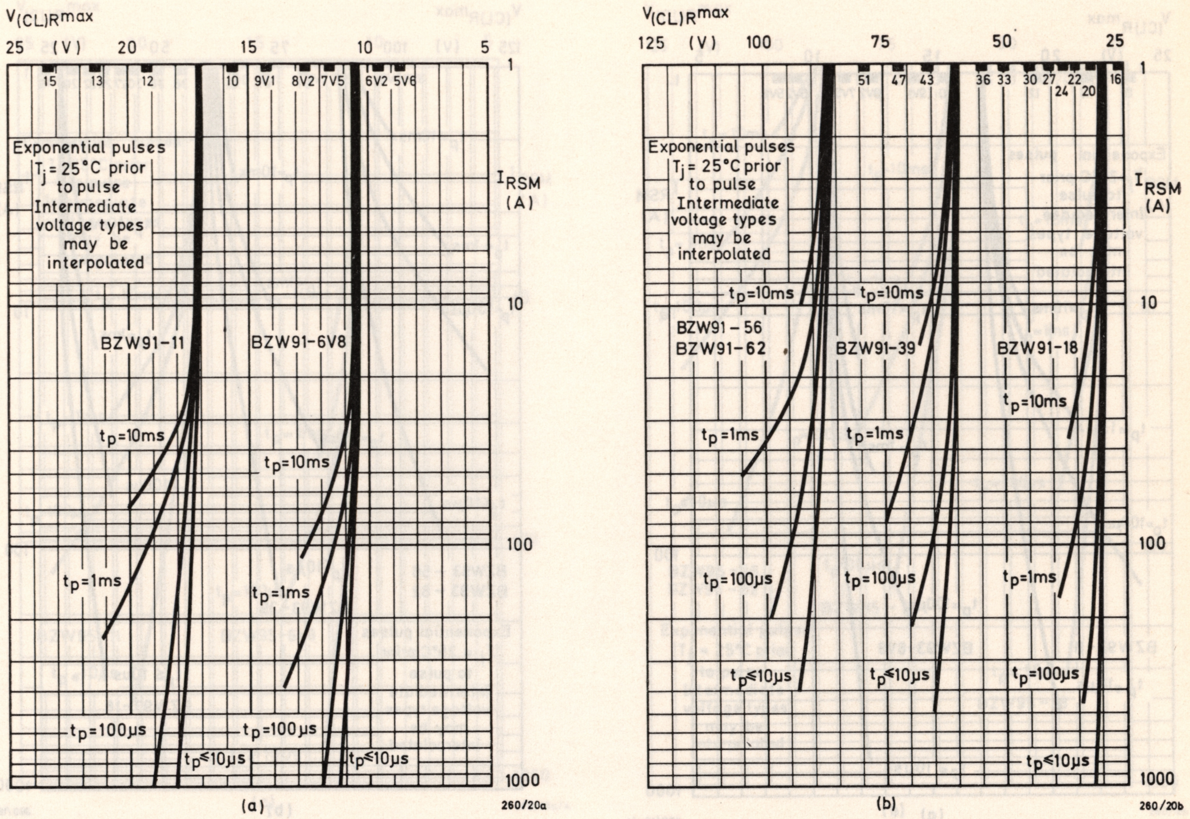

Fig. 20—Non-repetitive reverse current against clamping voltage for step-and-exponential-decay pulses, BZW91 series (a) $V_{(CL)R}$ = 5 to 25V (b) $V_{(CL)R}$ = 25 to 125V

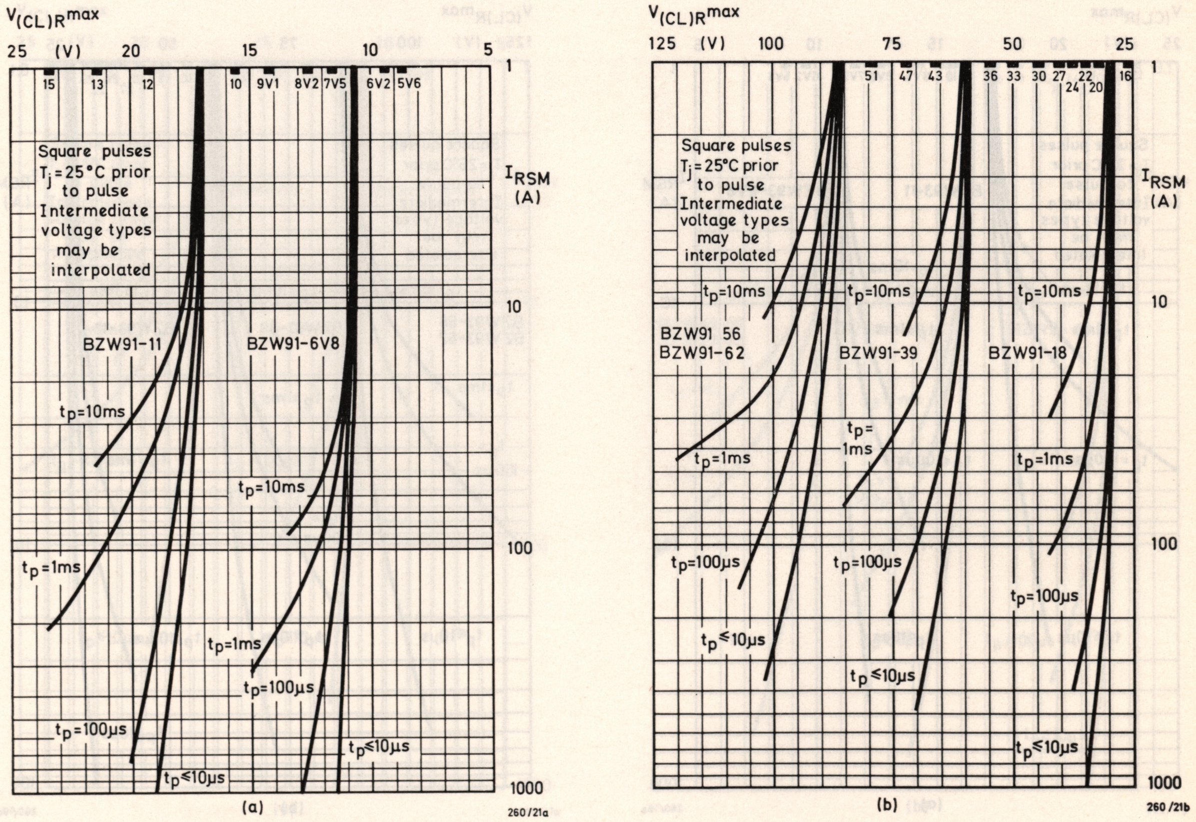

Fig. 21—Non-repetitive reverse current against clamping voltage for squarewave pulses, BZW91 series (a) $V_{(CL)R}$ = 5 to 25V (b) $V_{(CL)R}$ = 25 to 125V

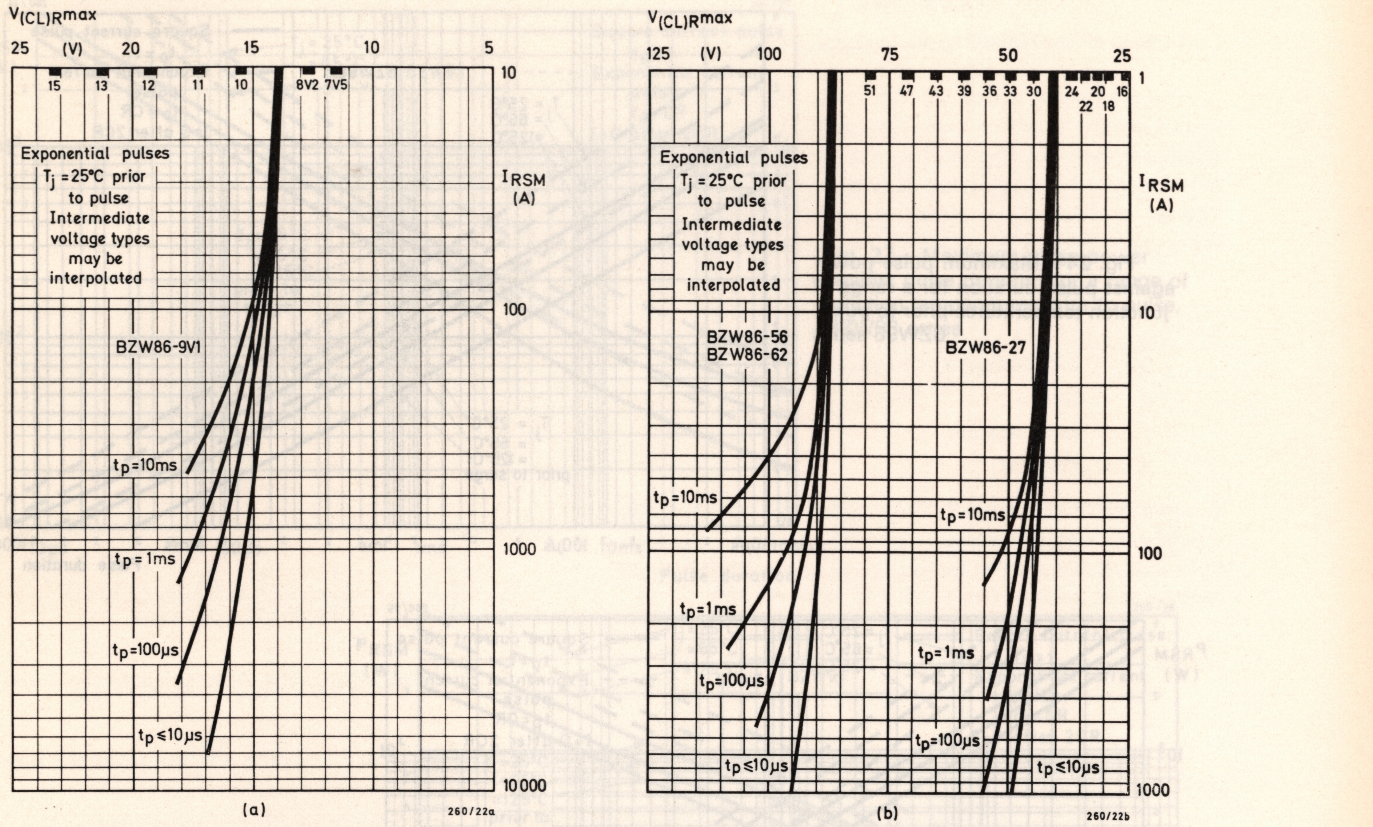

Fig. 22—Non-repetitive reverse current against clamping voltage for step-and-exponential-decay pulses, BZW86 series (a) $V_{(CL)R}$ = 5 to 25V (b) $V_{(CL)R}$ = 25 to 125V

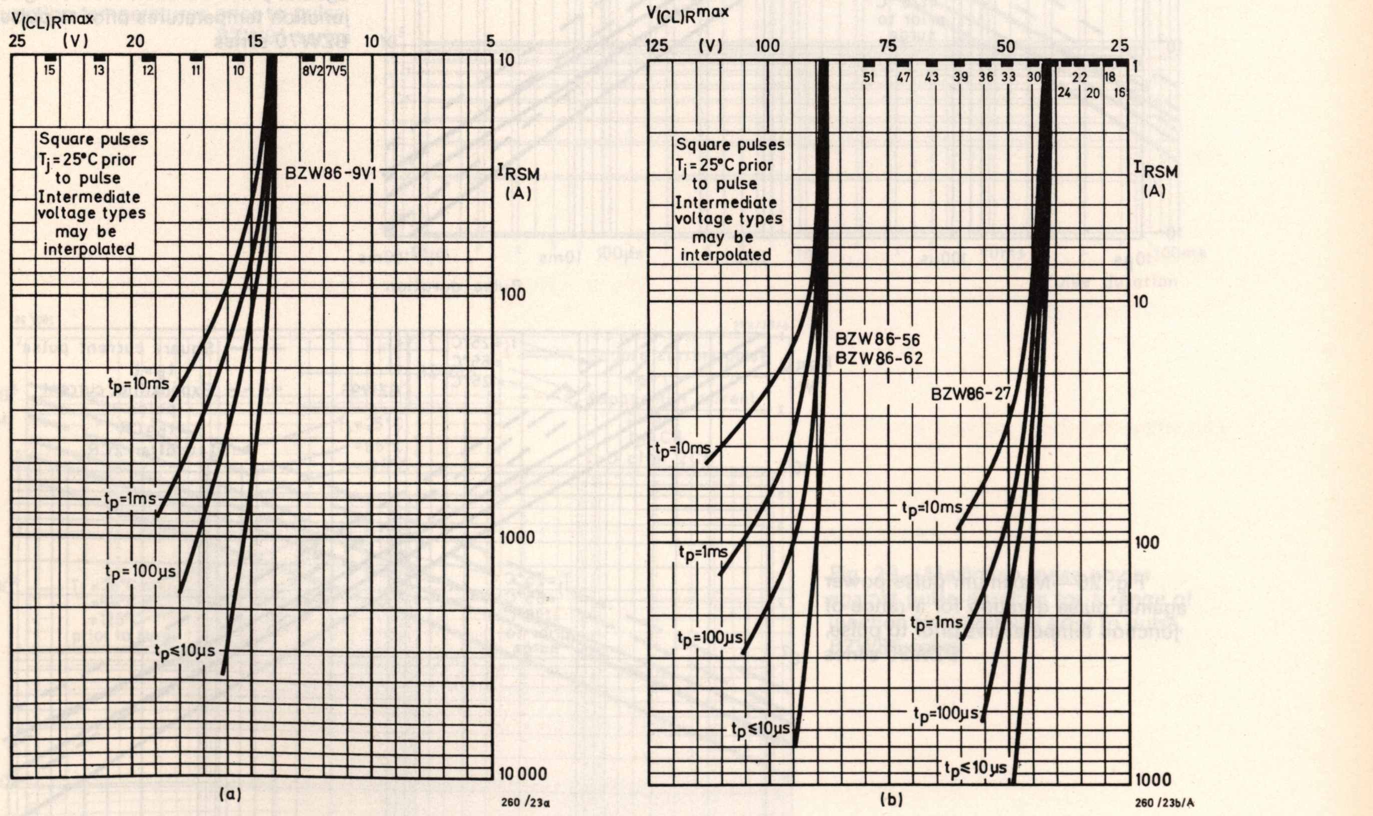

Fig. 23—Non-repetitive reverse current against clamping voltage for squarewave pulses, BZW86 series (a) $V_{(CL)R}$ = 5 to 25V (b) $V_{(CL)R}$ = 25 to 125V

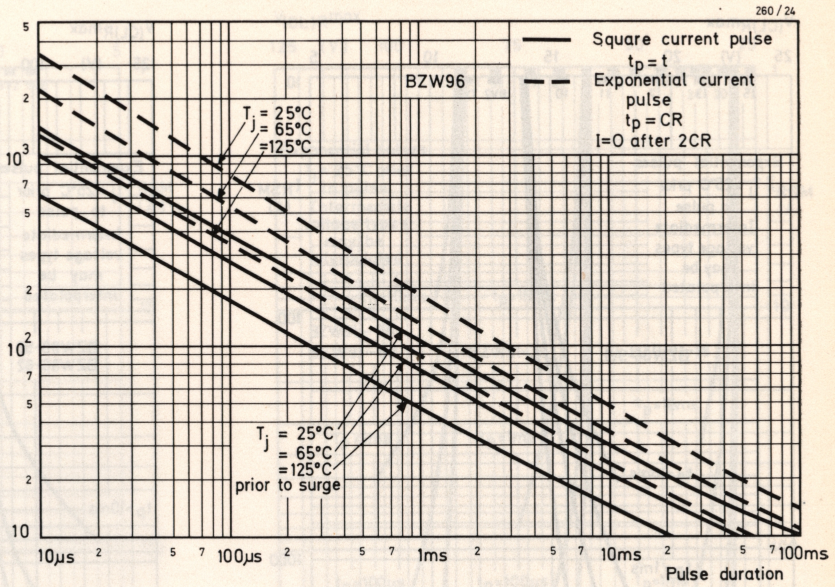

Fig. 24—Maximum pulse power against pulse duration for a range of junction temperatures prior to pulse, BZW96 series

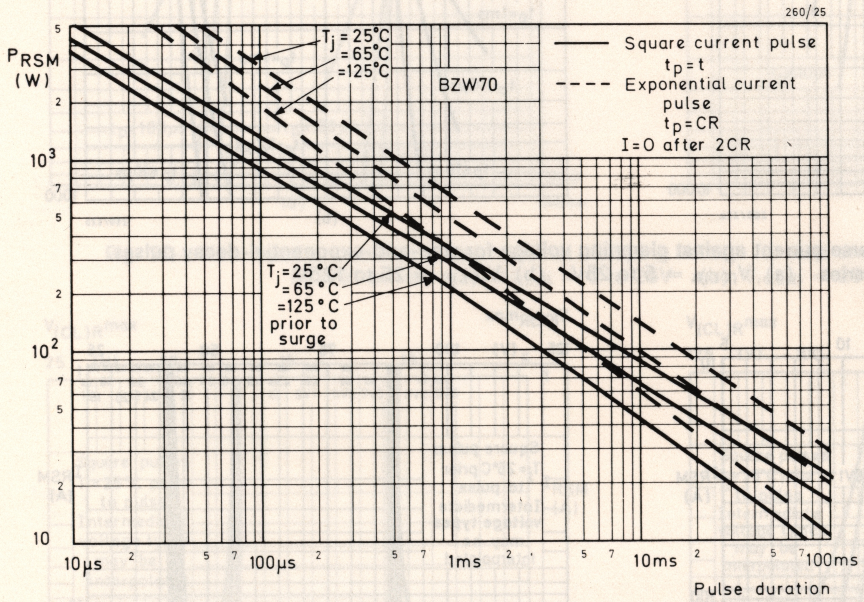

Fig. 25—Maximum pulse power against pulse duration for a range of junction temperatures prior to pulse, BZW70 series

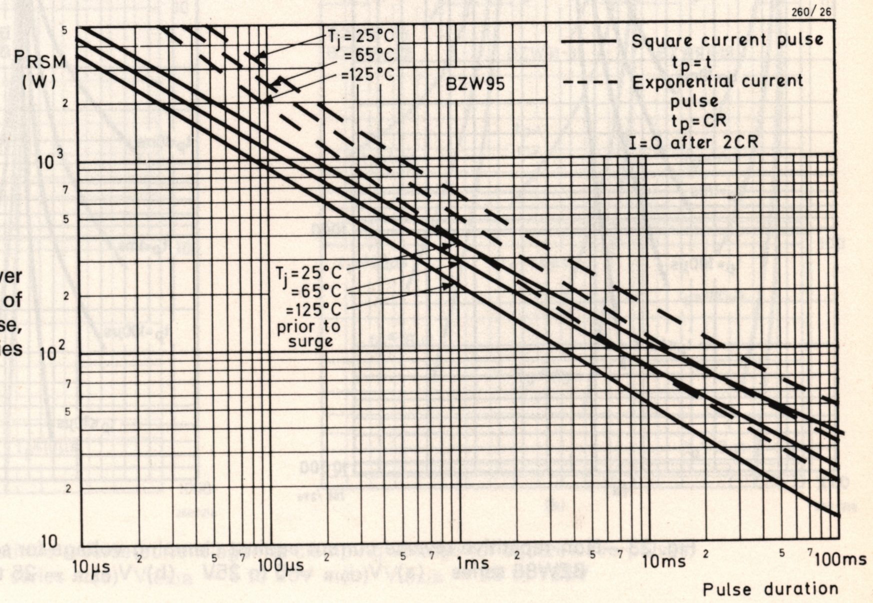

Fig. 26—Maximum pulse power against pulse duration for a range of junction temperatures prior to pulse, BZW95 series

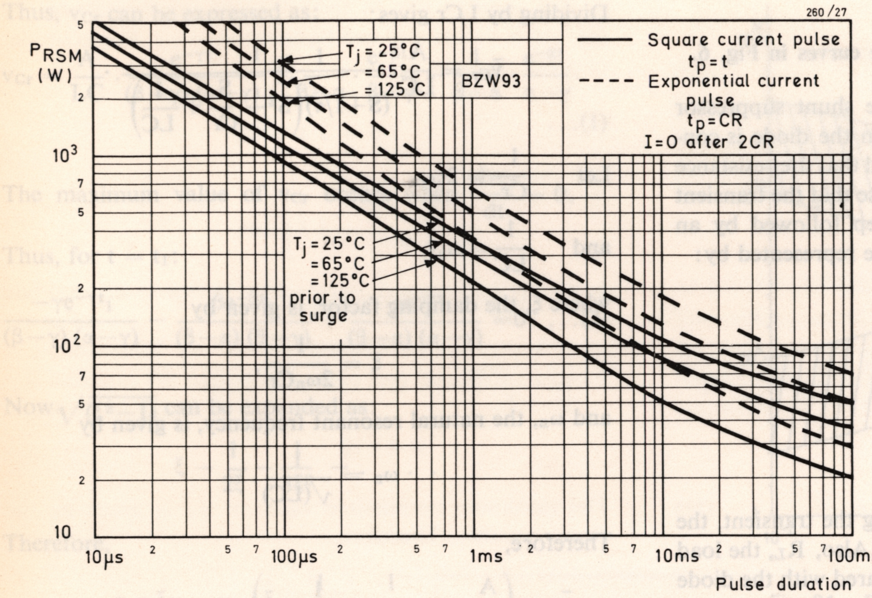

Fig. 27—Maximum pulse power against pulse duration for a range of junction temperatures prior to pulse, BZW93 series

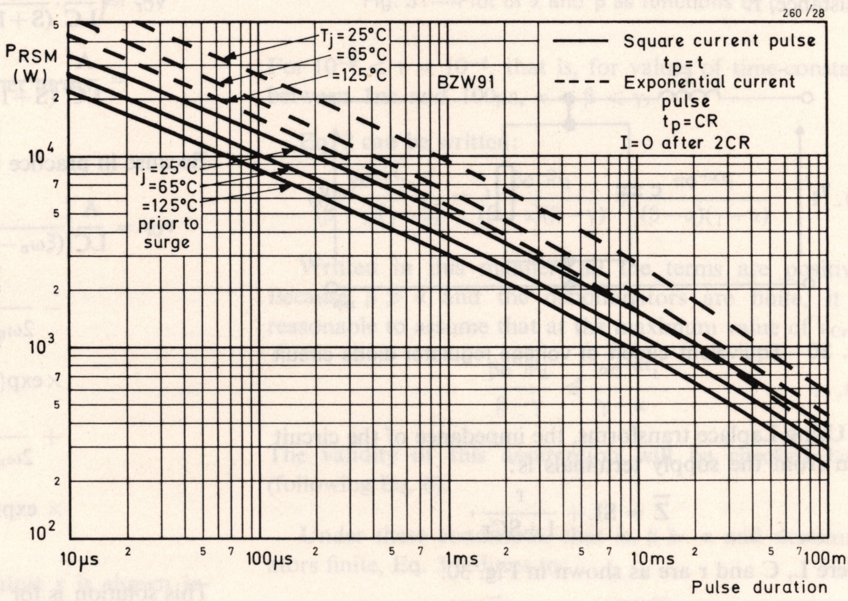

Fig. 28—Maximum pulse power against pulse duration for a range of junction temperatures prior to pulse, BZW91 series

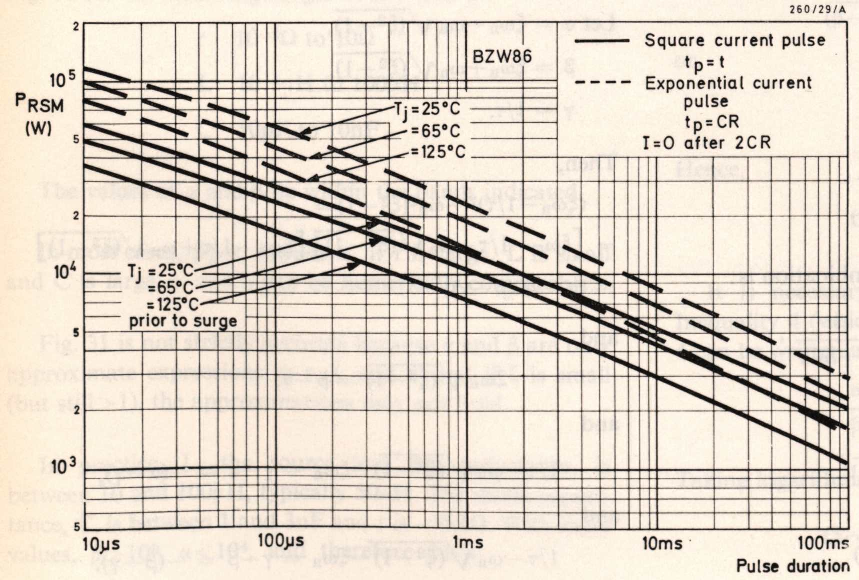

Fig. 29—Maximum pulse power against pulse duration for a range of junction temperatures prior to pulse, BZW86 series

APPENDIX

Derivation of normalised excess voltage curves in Fig. 6.

The equivalent circuit of the diode shunt suppressor circuit for the transient condition when the diode is conducting is shown in Fig. 30. It is assumed that the resistance of the supply is negligibly small. Suppose that the transient voltage applied to the circuit is a step followed by an exponential decay (Fig. 5) which can be represented by:

$$V_{St} = Ae^{-t/\tau},$$

where

V_{St} = instantaneous voltage
t = time
τ = time-constant
A = constant.

Because the diode conducts only during the transient, the steady-state supply voltage is ignored. Also, R_L, the load resistance, is assumed to be large compared with the diode resistance, r.

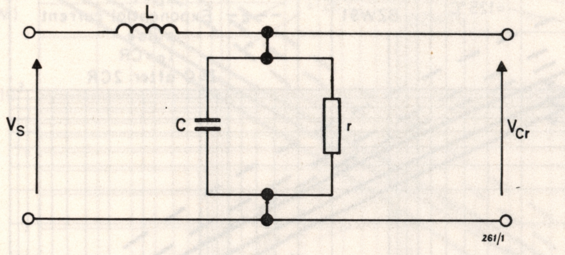

Fig. 30—Equivalent circuit of voltage regulator diode circuit

Using Laplace transforms, the impedance of the circuit seen from the supply terminals is:

$$\overline{Z} = SL + \frac{r}{1+SCr},$$

where L, C and r are as shown in Fig. 30.

The input voltage is:

$$\overline{v} = \frac{A}{S+1/\tau}.$$

Therefore, the input current is:

$$\overline{i} = \frac{A}{S+1/\tau}\cdot\frac{1}{SL+\dfrac{r}{1+SCr}},$$

and the voltage across the parallel Cr combination is:

$$\overline{v}_{Cr} = \frac{A}{S+1/\tau}\cdot\frac{1}{SL+\dfrac{r}{1+SCr}}\cdot\frac{r}{1+SCr},$$

$$= \frac{Ar}{(S+1/\tau)[SL(1+SCr)+r]},$$

$$= \frac{Ar}{(S+1/\tau)(S^2LCr+SL+r)}.$$

Dividing by LCr gives:

$$\overline{v}_{Cr} = \frac{A}{LC}\cdot\frac{1}{(S+1/\tau)\left(S^2+\dfrac{S}{Cr}+\dfrac{1}{LC}\right)}.$$

Let $\quad \dfrac{1}{Cr} = 2\xi\omega_n$

and $\quad \dfrac{1}{LC} = \omega_n^2$

where ξ, the damping factor, is given by

$$\xi = \frac{1}{2\omega_n Cr},$$

and ω_n, the natural resonant frequency, is given by

$$\omega_n = \frac{1}{\sqrt{(LC)}}.$$

Therefore,

$$\overline{v}_{Cr} = \frac{A}{LC}\cdot\frac{1}{(S+1/\tau)(S^2+2\xi\omega_n S+\omega_n^2)},$$

$$= \frac{A}{LC}\cdot\frac{1}{(S+1/\tau)[(S+\xi\omega_n)^2-\omega_n^2(\xi^2-1)]}.$$

Because in practice $\xi > 1$, the solution takes the form:

$$v_{Cr} = \frac{A}{LC}\left\{\frac{1}{(\xi\omega_n-1/\tau)^2-\omega_n(\xi^2-1)}\cdot e^{-t}/\tau - \right.$$

$$- \frac{1}{2\omega_n\sqrt{(\xi^2-1)}[1/\tau-\omega_n\sqrt{(\xi^2-1)}-\xi\omega_n]} \times$$

$$\times \exp\{-[\xi\omega_n+\omega_n\sqrt{(\xi^2-1)}]t\} +$$

$$+ \frac{1}{2\omega_n\sqrt{(\xi^2-1)}[1/\tau+\omega_n\sqrt{(\xi^2-1)}-\xi\omega_n]} \times$$

$$\times \exp\{-[\xi\omega_n-\omega_n\sqrt{(\xi^2-1)}]t\}.$$

This solution is for the overdamped case.

Let $\alpha = \xi\omega_n-\omega_n\sqrt{(\xi^2-1)}$,
$\beta = \xi\omega_n+\omega_n\sqrt{(\xi^2-1)}$,
$\gamma = 1/\tau$.

Then,

$$(\xi\omega_n-1/\tau)^2-\omega_n^2(\xi^2-1) =$$

$$= \left[\xi\omega_n-1/\tau-\omega_n\sqrt{(\xi^2-1)}\right]\left[\xi\omega_n-1/\tau+\omega_n\sqrt{(\xi^2-1)}\right]$$

$$= (\alpha-\gamma)(\beta-\gamma),$$

and

$$2\omega_n\sqrt{(\xi^2-1)} = \beta-\alpha,$$

and

$$1/\tau+\omega_n\sqrt{(\xi^2-1)}-\xi\omega_n = \gamma-\alpha = -(\alpha-\gamma),$$

and

$$1/\tau-\omega_n\sqrt{(\xi^2-1)}-\xi\omega_n = \gamma-\beta = -(\beta-\gamma).$$

Thus, v_{Cr} can be expressed as:

$$v_{Cr} = \frac{A}{LC}\cdot\frac{e^{-\gamma t}}{(\beta-\gamma)(\alpha-\gamma)} + \frac{1}{\beta-\alpha}\cdot\frac{e^{-\beta t}}{\beta-\gamma} - \frac{1}{\beta-\alpha}\cdot\frac{e^{-\alpha t}}{\alpha-\gamma}. \quad \ldots(1)$$

The maximum value of v_{Cr} occurs when $\dfrac{dv_{Cr}}{dt} = 0$.

Thus, for $t = t_1$:

$$\frac{-\gamma e^{-\gamma t_1}}{(\beta-\gamma)(\alpha-\gamma)} - \frac{\beta e^{-\beta t_1}}{(\beta-\alpha)(\beta-\gamma)} + \frac{\alpha e^{-\alpha t_1}}{(\beta-\alpha)(\alpha-\gamma)} = 0. \quad \ldots(2)$$

Now $\sqrt{(\xi^2-1)}$ can be expanded as:

$$\xi - \frac{1}{2\xi} - \frac{1}{8\xi^3} - \ldots.$$

Therefore,

$$\alpha = \xi\omega_n - \omega_n\left(\xi - \frac{1}{2\xi} - \frac{1}{8\xi^3} - \ldots\right).$$

When $\xi \gg 1$, ignoring cubic and higher terms,

$$\alpha \simeq \frac{\omega_n}{2\xi}.$$

Under the same condition,

$$\beta \simeq 2\xi\omega_n.$$

Therefore,

$$\alpha \simeq \frac{r}{L},$$

and,

$$\beta \simeq \frac{1}{Cr}.$$

A diagram of α and β plotted against r is shown in Fig. 31 for the following ranges of r, L and C.

r $10^{-2}\Omega$ to 10Ω
L $10^{-1}\mu$H to 100μH
C 10pF to 10nF

The values of α and β lie within the bands indicated.

In most cases, $\beta \gg \alpha$. However, if r is large, L is small and C is large, α and β can be numerically comparable.

Fig. 31 is not strictly accurate because α and β are only approximate expressions in r, L and C and if ξ is small (but still >1), the approximations may not hold.

In practice, L, the source and line inductance, is between 10 and 100μH, typically 50μH. The diode capacitance, C, is between 1 and 3nF and r is $<0.1\Omega$. With these values, $\beta > 10^9$, $\alpha < 10^4$, and therefore $\beta \gg \alpha$.

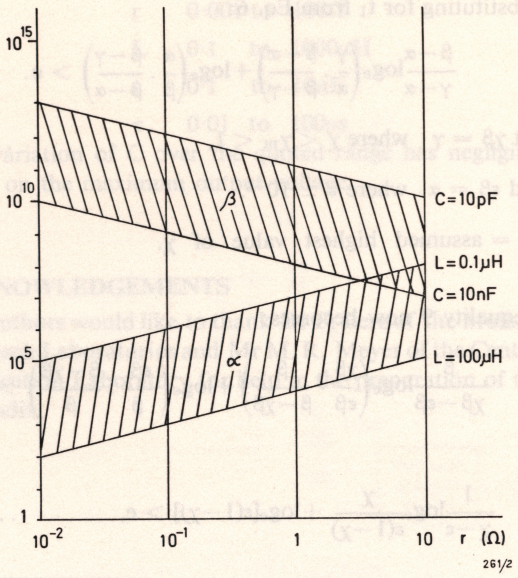

Fig. 31—Plot of α and β as functions of r

For $10^{-9} < \tau < 10^{-4}$, that is, for values of time-constant between 1ns and 100μs, $\alpha < \beta < \gamma$.

Eq. 2 can be written:

$$\frac{\gamma e^{-\gamma t_1}}{(\beta-\gamma)(\gamma-\alpha)} = \frac{\beta e^{-\beta t_1}}{(\beta-\alpha)(\beta-\gamma)} + \frac{\alpha e^{-\alpha t_1}}{(\beta-\alpha)(\gamma-\alpha)}. \quad \ldots(3)$$

Written in this manner, all the terms are positive. Because $\beta \gg \alpha$ and the denominators are finite, it is reasonable to assume that at the maximum value of v_{Cr}

$$\frac{\beta e^{-\beta t_1}}{\beta-\gamma} \ll \frac{\alpha e^{-\alpha t_1}}{\gamma-\alpha}. \quad \ldots(4)$$

The validity of this assumption will be checked later (following Eq. 6).

Under these conditions, that is, $\beta \gg \alpha$ and denominators finite, Eq. 3 reduces to:

$$\frac{\gamma e^{-\gamma t_1}}{(\beta-\gamma)(\gamma-\alpha)} = \frac{\alpha e^{-\alpha t_1}}{(\beta-\alpha)(\gamma-\alpha)},$$

or,

$$e^{(\gamma-\alpha)t_1} = \frac{\gamma}{\alpha}\cdot\frac{\beta-\alpha}{\beta-\gamma}. \quad \ldots(5)$$

Hence,

$$t_1 = \frac{1}{\gamma-\alpha}\log_e\left(\frac{\gamma}{\alpha}\cdot\frac{\beta-\alpha}{\beta-\gamma}\right). \quad \ldots(6)$$

It is necessary to check the conditions for which Inequality 4 (which leads to Eq. 6) is justified. Inequality 4 can be written as:

$$\frac{\alpha}{\beta}\cdot\frac{\beta-\gamma}{\beta-\alpha}\cdot e^{(\beta-\alpha)t_1} \gg 1. \quad \ldots(7)$$

Taking logarithms of both sides:

$$(\beta-\alpha)t_1 + \log_e\left(\frac{\alpha}{\beta}\cdot\frac{\beta-\gamma}{\beta-\alpha}\right) > e. \quad \ldots(8)$$

Substituting for t_1 from Eq. 6:

$$\frac{\beta-\alpha}{\gamma-\alpha}\log_e\left(\frac{\gamma}{\alpha}\cdot\frac{\beta-\alpha}{\beta-\gamma}\right)+\log_e\left(\frac{\alpha}{\beta}\cdot\frac{\beta-\gamma}{\beta-\alpha}\right) > e. \quad \ldots(9)$$

Let $\chi\beta = \gamma$ where $\chi < \chi_m < 1$, $\quad\ldots(10)$

and $\varepsilon\beta = \alpha$ where $\varepsilon \simeq 10^{-4}$.

χ_m = assumed highest value of χ.

Inequality 9 now becomes:

$$\frac{\beta}{\chi\beta-\varepsilon\beta}\log_e\left(\frac{\chi\beta}{\varepsilon\beta}\cdot\frac{\beta}{\beta-\chi\beta}\right)+\log_e\left(\frac{\varepsilon\beta}{\beta}\cdot\frac{\beta-\chi\beta}{\beta}\right) > e,$$

or,

$$\frac{1}{\chi-\varepsilon}\log_e\frac{\chi}{\varepsilon(1-\chi)}+\log_e[\varepsilon(1-\chi)] > e, \quad\ldots(11)$$

or,

$$\frac{1}{\chi-\varepsilon}\log_e\frac{\chi}{\varepsilon}-\frac{1}{\chi-\varepsilon}\log_e(1-\chi)+\log_e(1-\chi)+\log_e\varepsilon > e. \quad\ldots(12)$$

For $\varepsilon < \chi < 1$,

$$\frac{-1}{\chi-\varepsilon}\log_e(1-\chi)+\log_e(1-\chi) > 0.$$

Therefore, Inequality 12 will be satisfied when:

$$\frac{1}{\chi-\varepsilon}\log_e\frac{\chi}{\varepsilon}+\log_e\varepsilon > e. \quad\ldots(13)$$

It can be shown that for $\chi > \varepsilon$, the term $\frac{1}{\chi-\varepsilon}\log_e\frac{\chi}{\varepsilon}$ decreases when χ is increased. Therefore Inequality 13 will be satisfied for $\chi < \chi_m$ if it is satisfied at $\chi = \chi_m$; that is, if,

$$\frac{1}{\chi_m-\varepsilon}\log_e\frac{\chi_m}{\varepsilon}+\log_e\varepsilon > e,$$

or,

$$\frac{1}{\frac{\chi_m}{\varepsilon}-1}\log_e\frac{\chi_m}{\varepsilon} > e\varepsilon-\varepsilon\log_e\varepsilon. \quad\ldots(14)$$

Consider a circuit with known values of α and β, and with γ as a variable parameter in a range $\alpha < \gamma < \gamma_m$ with $\gamma_m < \beta$. The maximum values of v_{Cr} will occur at $t = t_1$ as given by Eq. 6 for all values of γ in the specified range, provided that Inequality 14 is satisfied. That is,

$$\frac{1}{\frac{\gamma_m}{\alpha}-1}\log_e\frac{\gamma_m}{\alpha} \geqslant e\frac{\alpha}{\beta}+\frac{\alpha}{\beta}\log_e\frac{\beta}{\alpha}, \quad\ldots(15)$$

where $\gamma_m = \chi_m\beta$ and $\alpha = \varepsilon\beta$.

The equality sign in Inequality 15 corresponds to the maximum values that can be ascribed to γ_m. For example, consider the case where:

$$\alpha = 10^5,$$
$$\beta = 3{\cdot}3\times10^9,$$

and therefore

$$\frac{\beta}{\alpha} = 3{\cdot}3\times10^4.$$

From Inequality 15, taking $e \simeq 3$,

$$\frac{1}{\frac{\gamma_m}{\alpha}-1}\log_e\frac{\gamma_m}{\alpha} \geqslant \frac{3\times10^5}{3{\cdot}3\times10^9}+\frac{10^5}{3{\cdot}3\times10^9}\log_e\frac{3{\cdot}3\times10^9}{10^5},$$
$$\geqslant 4\times10^{-4}.$$

The maximum permissible value of γ_m is given by the above equality. Therefore,

$$\log_e\left(\frac{\gamma_m}{\alpha}\right)^{\left(\frac{1}{\frac{\gamma_m}{\alpha}-1}\right)} = 4\times10^{-4},$$

or,

$$\left(\frac{\gamma_m}{\alpha}\right)^{\left(\frac{1}{\frac{\gamma_m}{\alpha}-1}\right)} = e^{4\times10^{-4}}.$$

This can be solved graphically to give:

$$\gamma_m = 2{\cdot}5\times10^4\alpha.$$

Thus, when β/α is large, as in this example,

$$(\gamma_m)_{\max} \simeq \beta.$$

Let $\quad \frac{\gamma_m}{\alpha}-1 = \frac{\beta}{\alpha}(1-\eta)$, where η is small.

Substituting in Inequality 15 gives:

$$\frac{1}{\frac{\beta}{\alpha}(1-\eta)}\log_e\frac{\gamma_m}{\alpha} > \frac{e\alpha}{\beta}+\frac{\alpha}{\beta}\log_e\frac{\beta}{\alpha}.$$

Therefore,

$$(1-\eta) = \frac{\log_e\frac{\gamma_m}{\alpha}}{\frac{\beta}{\alpha}\left(e\frac{\alpha}{\beta}+\frac{\alpha}{\beta}\log_e\frac{\beta}{\alpha}\right)} = \frac{\log_e\frac{\gamma_m}{\alpha}}{e+\log_e\frac{\beta}{\alpha}},$$

and

$$\eta = 1-\frac{\log_e\frac{\gamma_m}{\alpha}}{e+\log_e\frac{\beta}{\alpha}},$$

$$= \frac{e+\log_e\frac{\beta}{\alpha}-\log_e\frac{\gamma_m}{\alpha}}{e+\log_e\frac{\beta}{\alpha}}.$$

Because $\beta \simeq \gamma_m$,

$$\eta \simeq \frac{e}{e+\log_e\frac{\beta}{\alpha}}.$$

Thus,

$$\left(\frac{\gamma_m}{\alpha}\right)_{\max} = \frac{\beta}{\alpha}\left(1-\frac{e}{e+\log_e\frac{\beta}{\alpha}}\right)+1, \quad\ldots(16)$$

and over the ranges of values taken, Inequality 4 and Eq. 6 are valid.

Solutions of Eq. 1 were determined for values of L, r, C and τ in the following ranges and the results plotted as shown in Fig. 6.

r	0·001	to	100Ω
L	0·1	to	1000μH
c	0·1	to	10nF
τ	0·01	to	100μs

The variation of C over the quoted range has negligible effect on the maximum output voltage.

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High-power broadband linear amplifiers using transistors type 810BLY/A

We regret that in this article certain parts of Figs. 2, 9 and 17 are incorrect. In particular, the 25Ω output balun in Fig. 2, the 50Ω input (bottom left) and 50Ω output baluns in Fig. 9, and the 25Ω, 50Ω balun in Fig. 17 are wrongly drawn. Revised versions of these three figures are given below and overleaf.

Corrections made

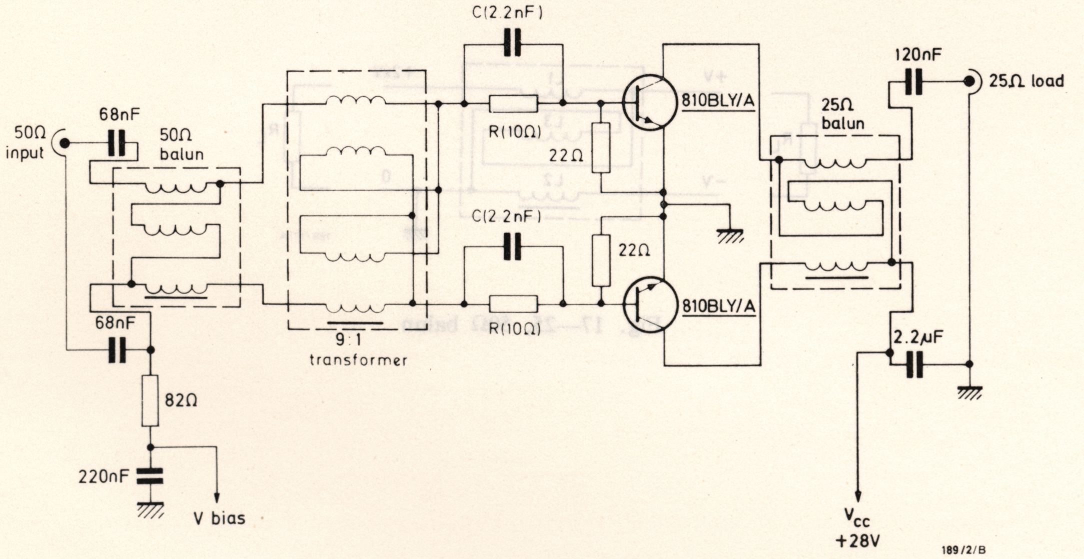

Fig. 2—50W p.e.p. amplifier circuit

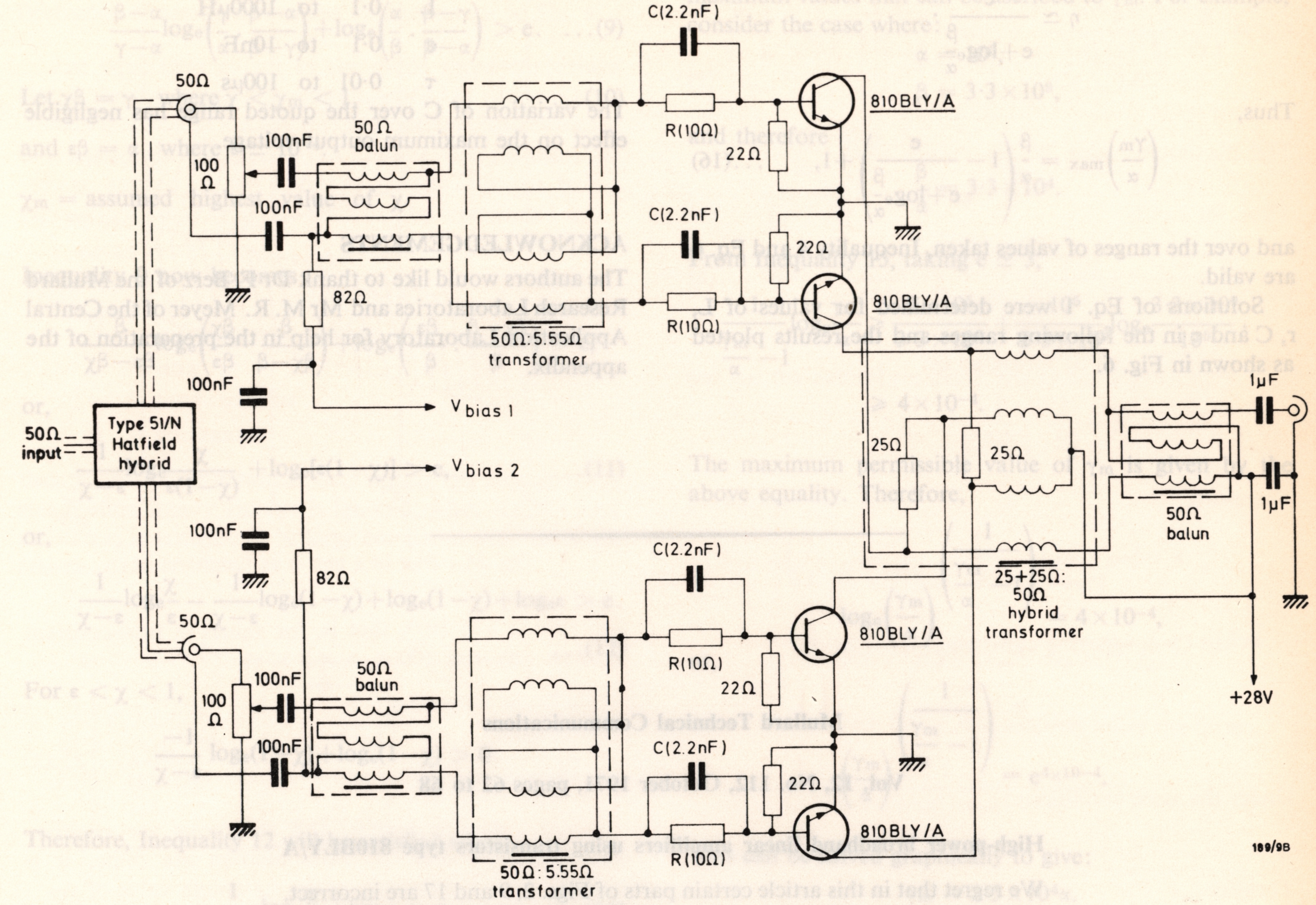
50Ω
100nF
50Ω balun
100 Ω
100nF
82Ω
100nF
C(2.2nF)
R(10Ω)
22Ω
810BLY/A
C(2.2nF)
22Ω
R(10Ω)
810BLY/A
50Ω:5.55Ω transformer
V bias 1
V bias 2
50Ω input
Type 51/N Hatfield hybrid
100nF
82Ω
50Ω
100 Ω
100nF
50Ω balun
100nF
C(2.2nF)
R(10Ω)
22Ω
810BLY/A
C(2.2nF)
22Ω
R(10Ω)
810BLY/A
50Ω:5.55Ω transformer
25Ω
25Ω
25+25Ω: 50Ω hybrid transformer
1µF
1µF
50Ω balun
+28V
189/9B

Fig. 9—100W p.e.p. amplifier circuit

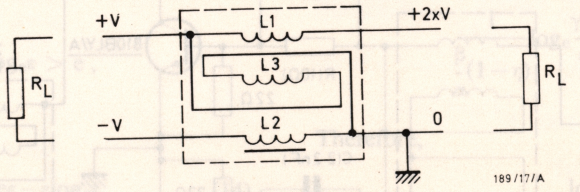
+V
R_L
L1
L3
L2
-V
+2xV
R_L
0
189/17/A

Fig. 17—25, 50Ω balun